1978

A microprocessor controller for an impulse generator.

Maria Kit-cham. Tam
University of Windsor

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A MICROPROCESSOR CONTROLLER FOR AN IMPULSE GENERATOR

by

Maria Kit-cham Tam

A Thesis
submitted to the Faculty of Graduate Studies
through the Department of
Electrical Engineering in Partial Fulfillment
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The University of Windsor

Windsor, Ontario, Canada

1978

ABSTRACT

A MICROPROCESSOR CONTROLLER

FOR AN IMPULSE GENERATOR

by

Maria Kit-cham Tam

This thesis describes the design and construction of a microprocessor-based controller for an impulse generator. A low cost hardware realization has been developed using the INTEL 4004 microprocessor and its associated architecture. The controller allows a number of experiments associated with high voltage breakdown phenomena to be completely automated. The design also interfaces with a transient digitizer and provides a capability for off-line data analysis. The controller has been tested by simulating the high voltage equipments normally connected to the microprocessor-based controller.

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FIGURE

NOMENCLATURE

A	sum of in_i
B	number of breakdown tests (in firmware); sum of i^2n_i (in diagnostic software)
BCD	binary-coded decimal
C	charging voltage
CCD	charged-coupled device
C^3L	complementary coincident current logic
CMOS	complementary MOS
CPU	central processing unit
D	incremental voltage
d	new incremental voltage
DMOS	double diffused MOS
DTL	diode-transistor logic
ECL	emitter-coupled logic
EFL	emitter-follower logic
i	sequential order
I^2L	integrated-injection logic
K	number of tests completed
M	sample size
MNOS	metal nitride oxide semiconductor
MOS	metal oxide semiconductor
MOSFET	metal oxide semiconductor field effect transistor
N	number of tests to be performed (in firmware); sum of n_i (in diagnostic software)
n_i	frequency at level y_i
NB	number of non-breakdown tests

NOMENCLATURE (Continued)

NMOS	n-channel MOS
p, F(z)	cumulative normal distribution function
PMOS	p-channel MOS
PROM	programmable read-only-memory
RAM	random-access-memory
RTL	resistor-transistor logic
S	estimate of standard deviation
S_s	estimate of standard deviation of S
$S_{\bar{y}}$	estimate of standard deviation of $\bar{y}$
$S_{\bar{y} + z_p s}$	estimate of standard deviation of $\bar{y} + z_p s$
S_σ	new estimate of standard deviation
SOS	silicon-on-sapphire
T	tolerance
$t_{\alpha/2, N-1}$	variable of t-distribution function
T^2L, TTL	transistor-transistor logic
T^2LS	transistor-transistor logic Schottky
VMOS	V-groove MOS
Y	initial charging voltage
$\bar{y}$	estimate of mean
y_i	subsequent levels
y_o	lowest level of symbol occurring less frequently
z, z_p	variable of normal distribution function
3D	triple diffused structures
α	confidence limit
u	mean
σ	standard deviation

CHAPTER ONE

INTRODUCTION

1.1. AUTOMATION OF IMPULSE TESTING

An impulse generator is found in most high voltage laboratories. Due to the nature of experiments, a set of tests usually involves repetitions of certain procedures many times in order to obtain sufficient data. Manual control of such experiments becomes inefficient and sometimes boring. The control system supplied with the impulse generator was found to be inadequate for the type of experiments planned at The University of Windsor high-voltage laboratory. It was thus necessary to design and construct a new control system which allows automatically charging the generator, triggering, detection of success or failure, self-adjustment based on some preset increment and recording of results. With such a system a researcher can devote more time to other intellectual work. Also human response time for each test is eliminated, which improves total time for completing the experiments.

Automation is best achieved by applying digital logic phenomenon because of simplicity and speed. At the present time realization of digital logic is accomplished either by discrete logic components or through programmability of microprocessors. Due to lower cost, faster speed, more compact size, higher flexibility and better reliability, it was decided to design a microprocessor-based system.

1.2. SUMMARY OF CHAPTERS

This thesis presents the design and construction of a micorprocessor-based automation system for an impulse generator. In Chapter Two the nature of an impulse generator and its use in a high-voltage laboratory are discussed. Overall description of system configurations is illustrated in this chapter.

Selection of microprocessor for this particular application and design constraints are presented in Chapter Three. Chapter Four is devoted to the description of the automated control system. This chapter gives detailed discussion on both hardware and software. The statistical method chosen is also included.

Experimental results obtained from simulation are provided in Chapter Five. This is followed by conclusions and suggestions of future work in Chapter Six. Listings of programs and a summarized procedure of operation are given in Appendices.

CHAPTER TWO

SYSTEM OVERVIEW

2.1. INTRODUCTION

Electric strength of equipments in an electric power system can be investigated by using impulse voltage testing procedure. The purpose of impulse tests is to ensure that various elements of an overhead line transmission system will give satisfactory service. They include tests to demonstrate that the flashover voltage of insulators and protective devices is not too low to cause unnecessary interruptions of supply; that the insulation of transformers, switchgears, cables etc. will withstand the highest voltages to which they may be subjected; and that protective gaps and other devices limit the voltage to a desired level and are not damaged by lightning current.

2.2. IMPULSE GENERATOR CIRCUIT

Lightning surges in general rise rapidly to a maximum value in a few microseconds and fall to a low value in a period approaching 100 microseconds. They can have a variety of wave-shapes with reversals of polarity. However, in most impulse testing laboratories, it has become the practice to use an impulse voltage wave which corresponds to the usual form of a travelling wave encountered on transmission lines. Occasionally other wave shapes of more extreme characteristics are used.

Various multi-stage impulse generators have been used to produce impulse waves. Figure 1 shows an eight-stage impulse generator. An impulse testing system in general consists of a multistage impulse generator, a wave shape control circuitry, a test piece and recording and measuring devices which are shown in Figure 2. This system can be simplified to an equivalent circuit of Figure 3.

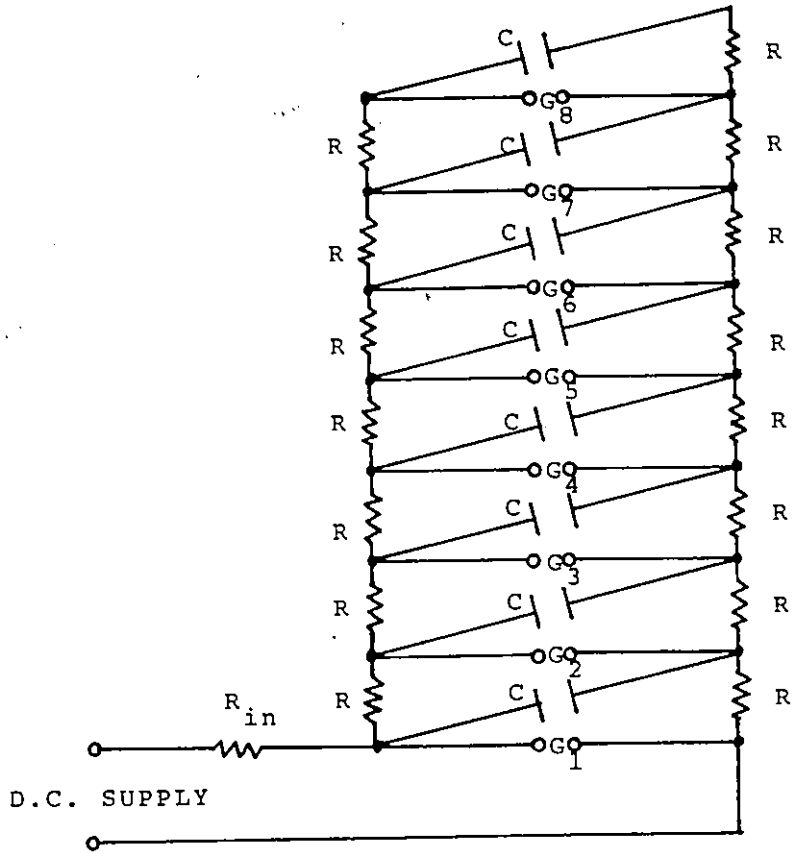


Figure 1. An eight-stage impulse generator

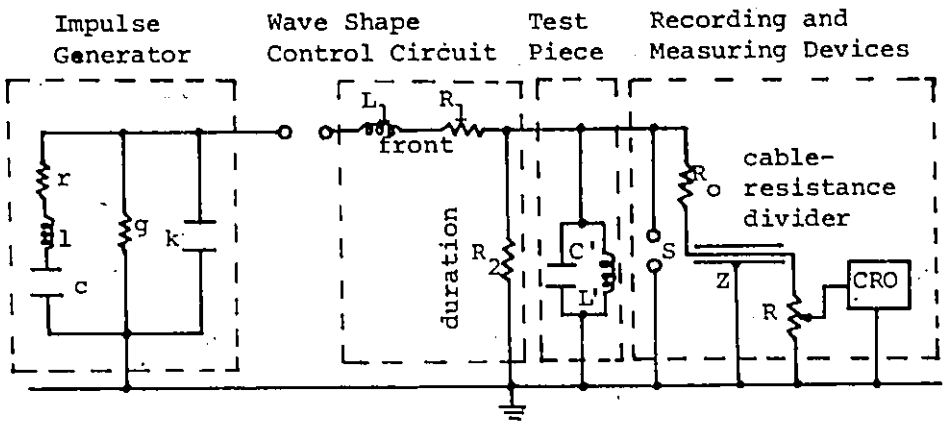


Figure 2. An impulse testing system

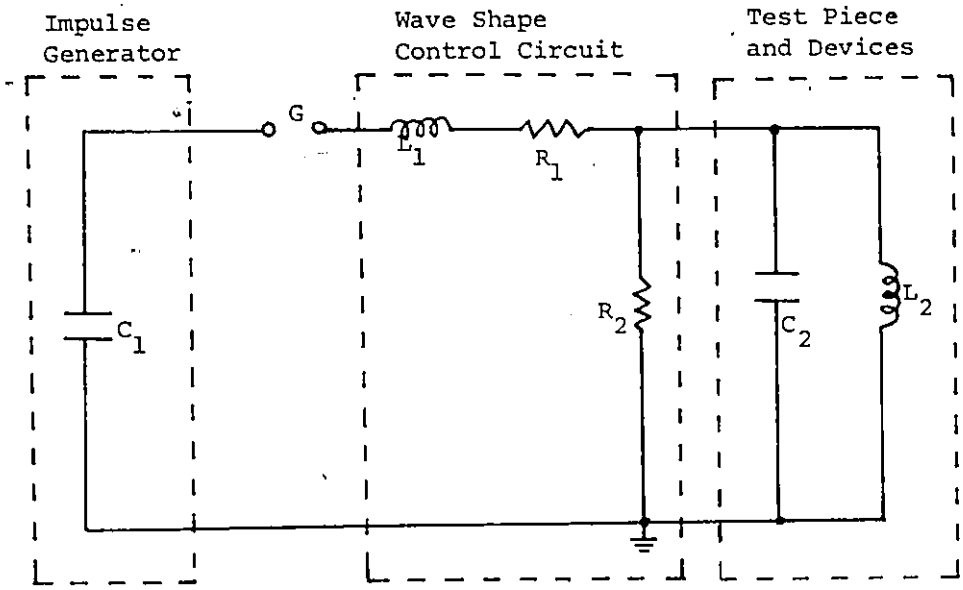


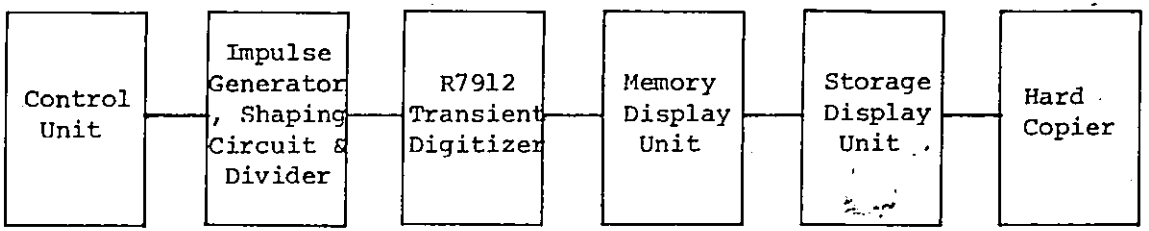
Figure 3. Equivalent circuit of impulse testing system

2.3. SYSTEM CONFIGURATIONS

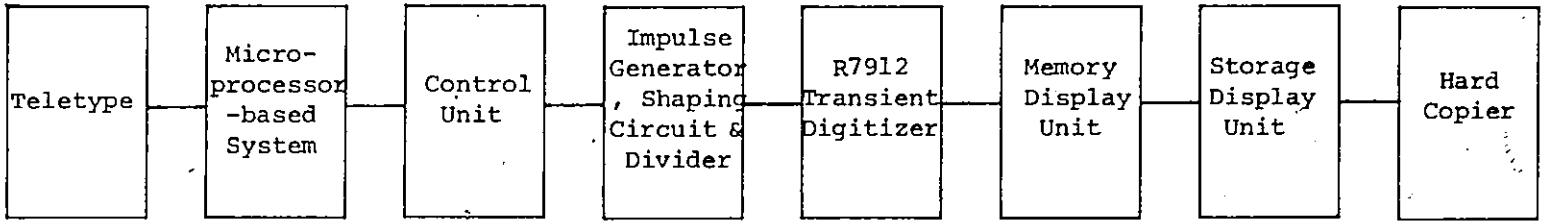
The high-voltage laboratory in The University of Windsor is equipped with a similar system described in last section. Operation of the system includes manually charging up generator, triggering the spark gap and recording results for each test. Through modification of this system with a microprocessor and appropriate interface, automation can be achieved. The microprocessor-based unit is designed on a cost-effective basis to such extent that necessary signals are provided with minimal changes of the original system. In this way manual control of the system may be used, if so desired.

Utilizing existing equipments, three different configurations can be set up for impulse testing. They are, as shown in Figure 4, manual, semi-automatic and fully automatic control. With the control unit switched to automatic the system can be operated semi- or fully automatically. Both operations are under the control of a central processing unit (CPU) which performs according to program prestored in programmable read-only-memory (PROM).

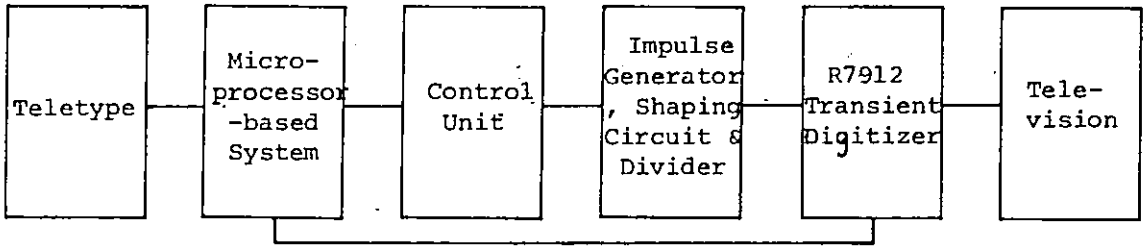
A user communicates with the CPU through a Teletype and the control and display panel. Specifications such as initial charging voltage, incremental voltage, number of tests, codes specifying semi- or fully automatic operation and delay before testing are accepted through the Teletype and stored in random-access-memory (RAM) for further processing. Results including indication of breakdown or



a. Manual operation



b. Semi-automatic operation



c. Fully automatic operation

Figure 4. System configurations for different operations

non-breakdown, subsequent charging voltage, number of tests performed and count of breakdown/non-breakdown occurrence are printed out and punched on paper tape as testing proceeds. Data in punched paper tape form are then read in and processed by a minicomputer system (NOVA 840) which has sufficient memory to perform statistical analysis on the results. In addition error messages are printed out when such condition is detected.

For fully automatic operation tests are carried out continuously without any outside intervention until completion or detection of fault. However the user may stop the process or reset the system any time by selecting the appropriate switches. In the case of semi-automatic operation, hard copies of output waveform displayed on the storage display unit can be obtained. This requires some manual control because of the features of the transient digitizer and its supporting equipments such as memory display unit, storage display unit and hard copier. Thus the CPU is brought to an idle state after each trial and continuation of the program is acquired only if READY switch is pushed. In this way sufficient time is provided for obtaining hard copies.

When malfunction of the system occurs, which may be due to faulty components, loose connections etc., in fully automatic operation that particular test is ignored and performed again. This is done at most five times. If such condition persists, error message is printed out and the program pointer is reset, whereas in the semi-automatic

operation it is interpreted as non-breakdown. However the output waveform displayed on the storage display unit reveals its actual condition. Hence special attention should be imposed when the system is operated semi-automatically.

CHAPTER THREE

DESIGN CONSIDERATIONS

3.1. CHOICE OF MICROPROCESSOR

In the selection of a microprocessor, the user is faced with understanding and comparing a myriad of parameters, such as cost, availability, programming aids, program checkout, architecture considerations, physical structure, second sourcing and testing. However timing played an important role in choosing a microprocessor specifically for this project. At the time when this project started, there existed only one microcomputer development system, namely the INTEL MCS-4, in the Department of Electrical Engineering of The University of Windsor. Naturally the microprocessor chosen was an INTEL 4004.

A central processor module —— IMM 4-42 of Figure 5 was then purchased from INTEL. This module contains the logic necessary to serve as a general purpose microcomputer. All the classic elements of a computer's architecture are assembled on the 6.18 x 8.0 inch card, including a 750 KHz crystal controlled system clock, control logic, a 4004 CPU, 320 words (4 bits) of read/write memory, memory control, four 4-bit input ports, eight 4-bit latching output ports, interface for standard ASR-33 Teletype and four sockets for 1K bytes of either 4001 mask programmed ROMs or 1702A erasable PROMs which contain appropriate program. Such a configuration

makes it adaptable to almost any requirement calling for the capabilities inherent in a microprocessor system and the hardware investment is minimal, which makes it quite favourable. This microprocessor may seem inferior in speed and memory addressed as compared to some of the other microprocessor, but it is adequate for this application where speed is not a crucial parameter.

3.2. DESIGN CONSTRAINTS

Since the design of the hardware is based on board level of a microcomputer, memory size is limited when minimal hardware investment is required. In this case only 1K bytes of PROM and 320 x 4 bits of RAM are available. Thus the software has to be as optimal as possible to include all required features. No redundancy in the software is allowed.

There are only four 4-bit input ports and eight 4-bit output ports. Expansion on the I/O ports is thus required when more ports are needed.

Since direct interface to the impulse generator is provided through the Control Unit, some of the control functions such as charging rate requirements are included in the Control Unit itself. The microprocessor-based unit is used to implement other functions which will be discussed in Chapter Four.

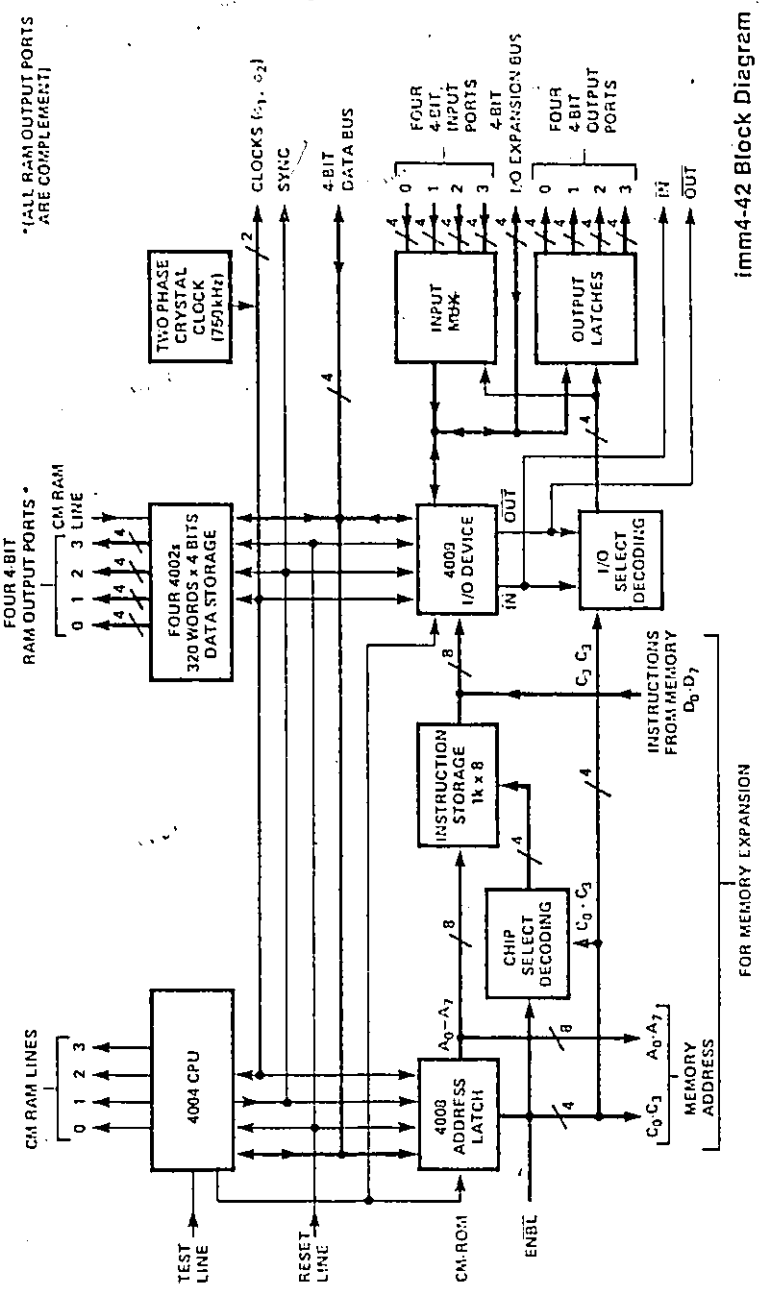


Figure 5. Central processor module

CHAPTER FOUR

A MICROPROCESSOR-BASED CONTROL SYSTEM FOR AN IMPULSE GENERATOR

4.1. INTRODUCTION

The automatic impulse testing system must provide various DC levels corresponding to the charging voltages. It must also monitors the position of the grounding arm, triggering at the spark gap and the measuring equipments. Additionally, the system must be able to distinguish breakdown and non-breakdown tests. Finally the system must be capable of accepting specifications and recording results. The microprocessor-based control system can accommodate these through co-ordination of hardware and firmware.

4.2. SYSTEM HARDWARE

The system hardware of the microprocessor-based controller consists of a central processor module and its interface, a control and display panel, and power supplies. A Teletype is used as input/output device.

4.2.a. THE BASIC SYSTEM

The central processor module is a quite complete system itself. The only external requirement is a DC power supply of +5 VDC and -10 VDC. However the input/output ports on the module is not sufficient for applying the module alone to controlling the whole impulse testing

system. An interface card is thus necessary for the expansion of input/output ports and other functions.

Figure 6 shows the basic block diagram of the system. All connections to the central processor module and the interface module are effected through two 100-pin, double-sided PC edge connectors. The interconnecting cables between the transient digitizer, memory display unit, storage display unit and hard copier are 104-, 25- and 13-lines. A 37-line cable is needed to link the transient digitizer with the microprocessor-based unit. The Teletype is tied to the system through an 8-pin connector. Coaxial cables and BNC connectors are used for other connections in the system. The power required by the central processor and interface modules is provided by two power supplies of ± 15 VDC, ± 1.2 ADC and +5 VDC, +6 ADC, -10 VDC, -3 ADC. The central processor module, the interface module, the power supplies and all required connectors are mounted on a chassis, which together with the front control and display panel form the microprocessor-based unit.

4.2.b. THE INTERFACE MODULE

The interface module is mainly made up of an input/output expansion and buffers section, digital-to-analog conversion section, flip-flops and lamp drivers section and Teletype interface section. A functional block diagram of the module is presented in Figure 7. Arrows indicate the direction of information transfer. The schematic diagram of

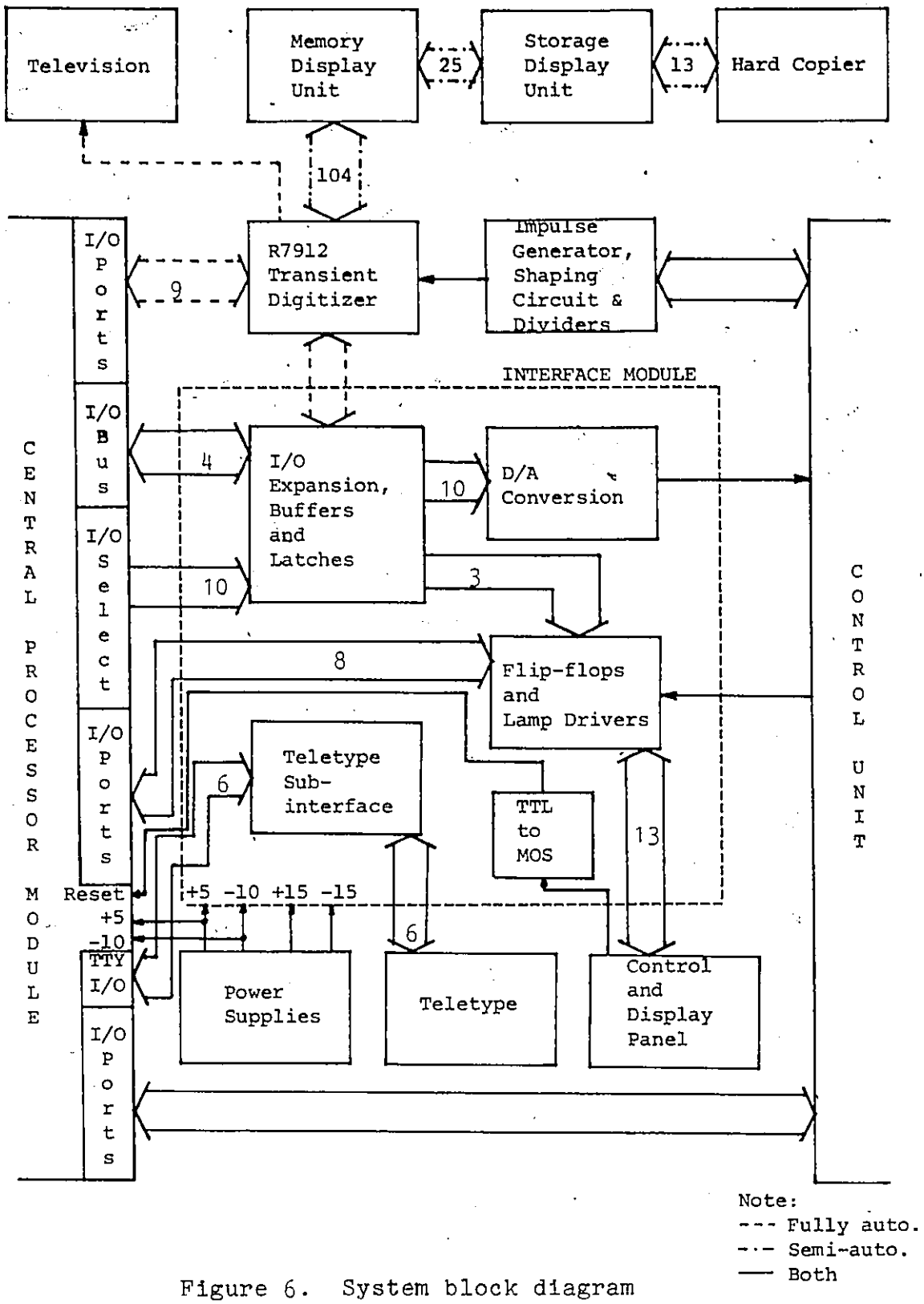


Figure 6. System block diagram

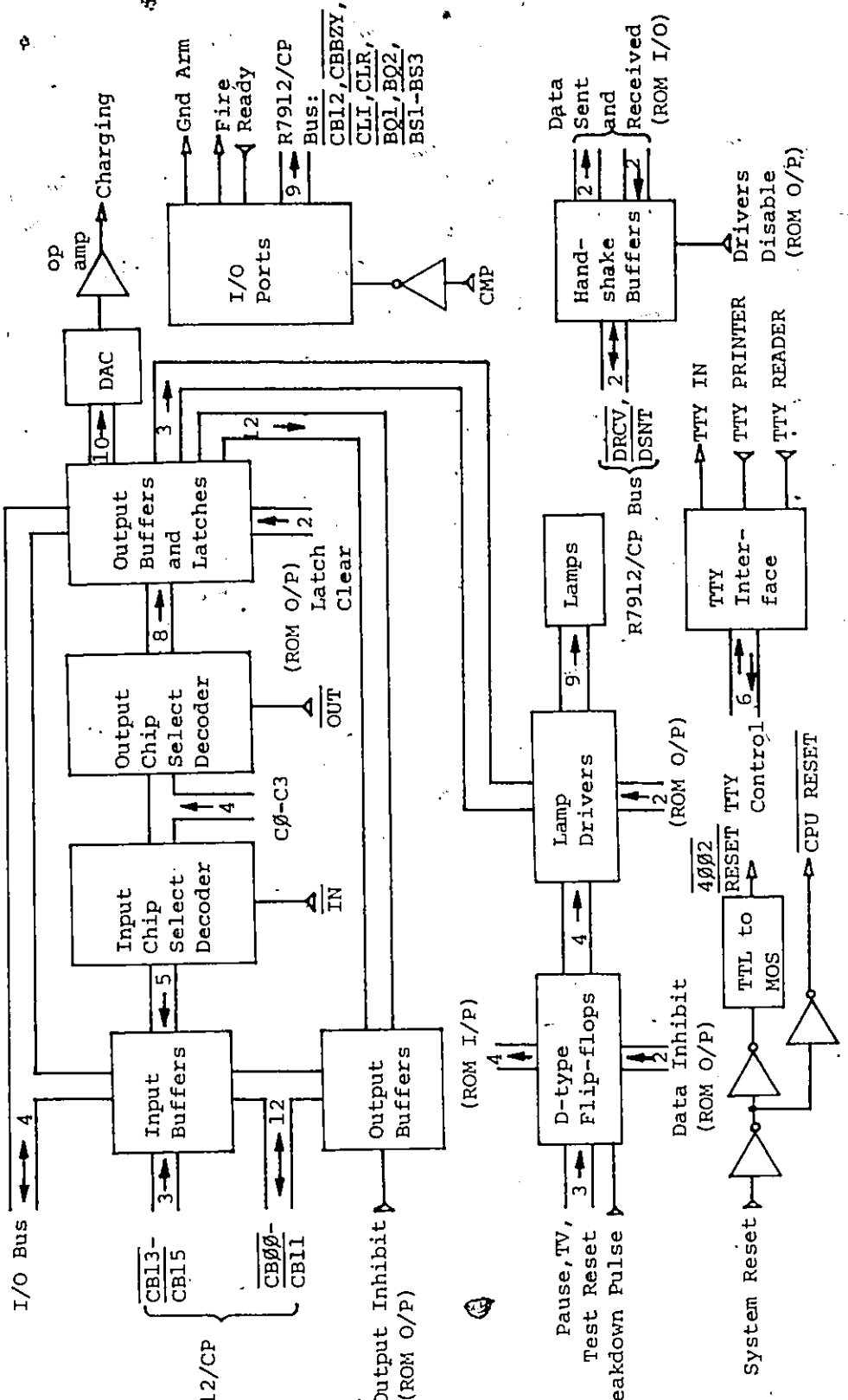


Figure 7. Functional block diagram of interface module

the module is shown in Figure 8.

Through decoding the appropriate signals, input ports can be expanded from four to sixteen and output ports from eight to forty-eight. Here only eight input and sixteen output ports are used. They are IROM Ø-3, 8-11, OROM Ø-3, 8-15 and RAM Ø-3. Two 74138 3-to-8 lines decoders are used to enable the input/output port that is chosen. The address of the port is represented in hexidecimal by the chip select CØ - C3. Hence the ports determined by this configuration are from #8 to #15. During an output operation $\overline{OUT}$ is low, and if the most significant bit of the port's address is high, then one of the decoders will be enabled, It decodes the states of CØ - C2 and set one of its eight output lines low. This in turn enables one of the four 74116 dual 4-bit latches and the content of the I/O bus is then latched to one of the eight output ports because output buffers are enabled by AND of C3 and OUT being high. This port will stay latched until it is overwritten by another output operation or the system is reset. Input operation is similar to output operation except that instead of $\overline{OUT}$, $\overline{IN}$ is used to enable the decoder and the content of one input port is then buffered to the I/O bus. Since 74126 tri-state buffers are used, the states of other input ports will not interfere with the operation. Also some of the lines, such as $\overline{CBØØ}$ - $\overline{CB11}$, $\overline{DRCV}$ and $\overline{DSNT}$, of the R7912 Digital-out bus are bidirectional, whereas the input/output ports of the

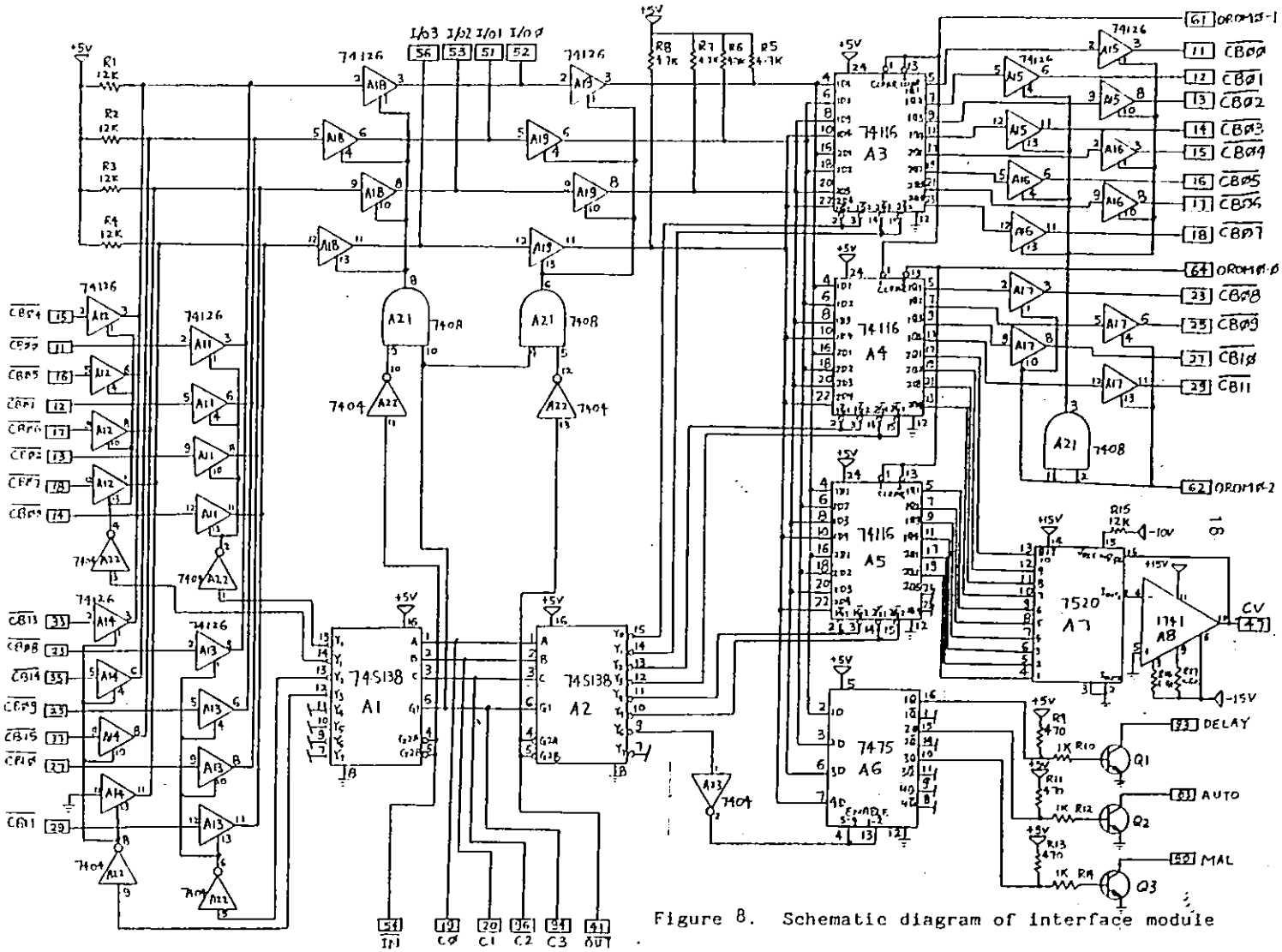


Figure 8. Schematic diagram of interface module

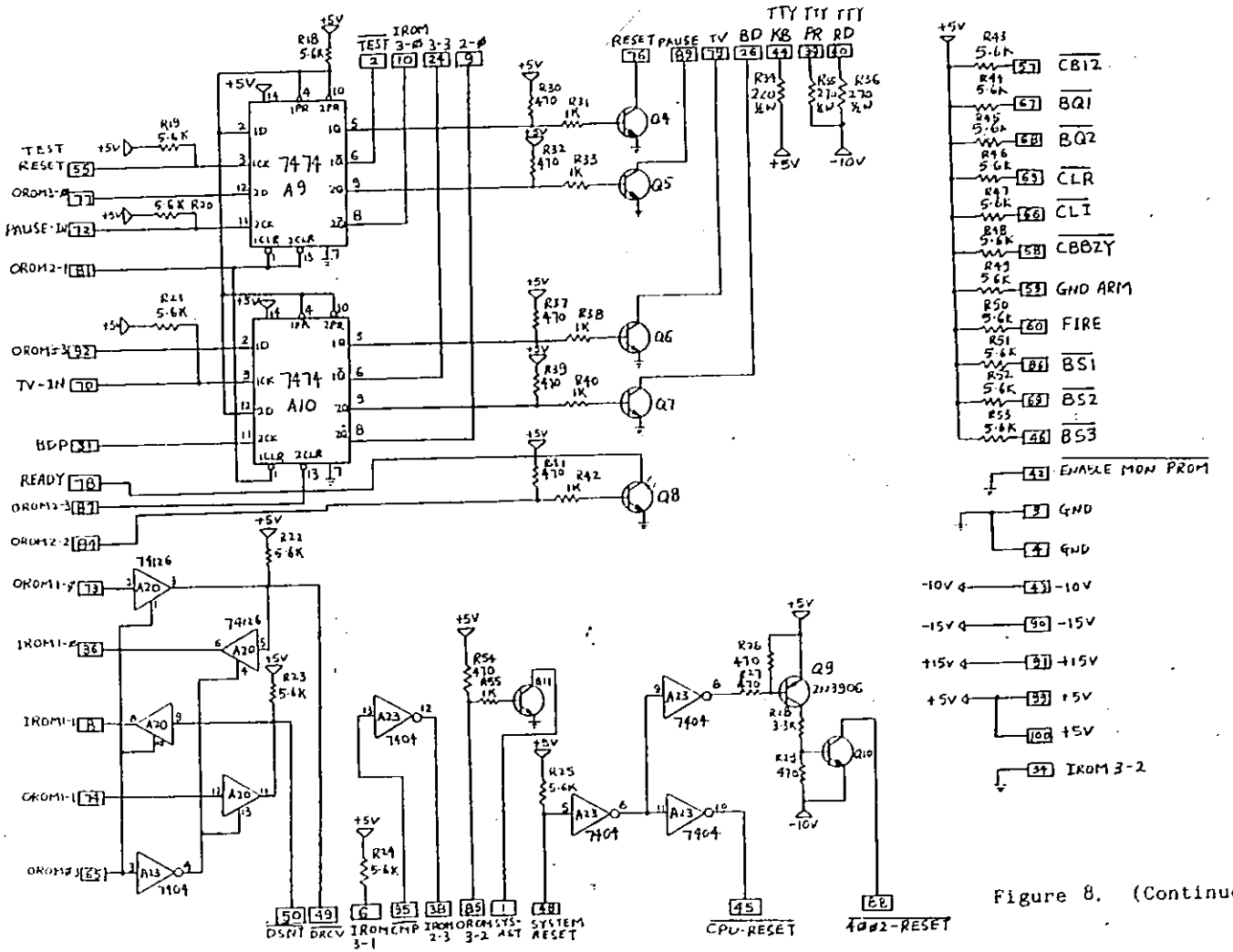


Figure 8. (Continued)

microprocessor-based system are unidirectional, thus tri-state buffers are used and the firmware program determines whether to enable or inhibit data transfer on each line. Through $\overline{\text{DSNT}}$-$\overline{\text{DRCV}}$ "handshake" the CPU communicates with the transient digitizer and proper sequence of operation is carried out by both units without loss of data.

A 10-bit D/A converter and an operational amplifier are employed to translate the digital representation of charging voltage in hexidecimal to a DC level within 0-5 V, which brings the actual charging voltage to a level within 0-100 KV. Hence resolution of charging voltage is .10 KV.

The switches at the front panel are lighted, single-pole, single throw. Action at the switches is recorded by D-type flip-flops. To avoid confusion by unnecessary lights, only those signals that require the attention of the operator are displayed. Due to current requirement of the lamps, current is amplified before applying to the lamps.

Two switches are provided for reset: TEST RESET and SYSTEM RESET. If SYSTEM RESET is pushed, the program counter is reset and the RAMs are cleared at that instant. To ensure that data is not misinterpreted in the following test and that system properly initialized TEST RESET should be used if the operator wishes to reset the system during the process of testing and after the generator is charged up. In such event program counter is set to zero after the trigatron is fired, charging voltage is set to zero and impulse generator is grounded. The $\overline{\text{CPU RESET}}$ pin on the processor chip enables

an operator to restart the program at any time. Execution following the $\overline{\text{CPU RESET}}$ always begins at program memory location zero. To obtain a complete reset of the CPU chip, the reset level must be maintained for a minimum of eight full instruction cycles, or 86.4 microsecond, to allow the index register refresh counter to scan all locations in memory. This refresh counter completes its scan of the chip every eight clock cycles, and a shorter $\overline{\text{CPU RESET}}$ would thus fail to clear the entire memory. The $\overline{\text{4ØØ2 RESET}}$ clears all data in RAM memory storage, including the memory cells, and the addressing registers. A minimum pulse width of 350 microsecond is required. Since 4ØØ2 RAMs require MOS level signals, the reset signal is converted from TTL to MOS level before it is applied to $\overline{\text{4ØØ2 RESET}}$ pin.

As discussed in Chapter 2, besides being operated in the fully automatic mode the system can be operated in semi-automatic mode, in which case the READY switch is used to provide sufficient time for obtaining hard copies and should be pushed after such action is completed for continuation of program. For fully automatic operation the display/digital mode can be altered through the TV switch during the process of testing. The PAUSE switch is for temporary stopping the process. It does not actually stop the program but the system is idled through looping of the program pointer at certain locations in the program until the PAUSE switch is pushed again. The occurrence of breakdown is recorded by triggering a flip-flop with the $\overline{\text{BDP-IN}}$ pulse

from the generator. Indicators such as DELAY, AUTO and MAL will be discussed in later section. Since the Central Processor Module has a built-in Teletype interface, the only additional requirements needed are three pull-up resistors.

It should be pointed out that the hardware configuration besides depending on the signals provided and required by the Central Processor Module, the Control Unit and the Transient Digitizer, also depends on the instruction set of the processor itself. It should be noted that there is no halt instruction and no interrupt facility. The only way to detect any external variation is through repeatedly scanning appropriate input ports. This is inefficient in both time and memory as compared to having an interrupt system. However for this particular control application of microprocessor time is not a crucial variable and the system can afford idling and routine scanning.

4.3. SYSTEM FIRMWARE

The system firmware is written in INTEL MCS-4 assembly language and electrically programmed on four 1702A EPROMs (1 K bytes) which are placed in the four sockets on the Central Processor Module. The control algorithm is shown in Figure 9 . Its main objective is to carry out impulse testings using "up-and-down", or "Bruceton", method.

4.3.a. APPLICATION OF "UP-AND-DOWN" METHOD

Basically the technique is to choose some initial charging voltage Y KV, interval between testing levels D KV

and sample size M. A succession of charging voltages is then used until M tests are completed. Subsequent charging level depends on the result of the preceding test. It is adjusted to -D KV below or +D KV above the level of the previous test, according to whether there was or was not a breakdown. The primary advantage of this method is that it automatically concentrates testing near the mean. In other words, for a given accuracy the "up-and-down" method requires fewer tests than the ordinary method of testing groups of equal size at preassigned levels. The saving in the number of observations may be of the order of 30 to 40 per cent.

To get a better estimate of the mean and improve concentration of observations around it, a rough search of the mean is incorporated in the algorithm. Starting with the level chosen by the operator, charging voltages of successive tests are decreased or increased unidirectionally by 10.0 KV depending on whether or not breakdown occurs until different condition occurs. Then the 50% point between the last breakdown and non-breakdown levels is used as the starting point for testing. For cases such as, if there is no breakdown even when the charging voltage is over 90.0 KV, testing starts at that level; or if breakdown keeps occurring and charging voltage is less than 10.0 KV, 5.0 KV will be chosen as the starting point. Since the maximum charging voltage is 100.0 KV, in this way a good starting point is obtained within two to ten observations. Inaccuracy by poor estimates of starting point and increment is thus reduced greatly.

4.3.b. THE ALGORITHM

The algorithm of the firmware in Figure 9 can be divided into four main parts: initializing output ports and loading specifications, setting up the system for testing, performing "up-and-down" procedure and detecting errors.

When the CPU is reset, all ROM output ports are high and RAM ports are low. They are then initialized to their proper states. Registers #8 and #9 are chosen as data RAM pointer. Starting from data RAM address Ø, eleven consecutive locations are used to store the first eleven decimal numbers input from the Teletype keyboard before 'carriage return' is typed, followed by nine locations for counters in decimal. Allocation of RAM is as follows:

$D_0D_1D_2$ - charging voltage C (.1 - 99.9 KV)

$D_3D_4D_5$ - incremental voltage D (.1 - 99.9 KV)

$D_6D_7D_8$ - sample size M (1 - 999)

D_9 - automatic option (=Ø - semi-automatic, ≠Ø - fully automatic)

D_A - delay option (=Ø - no delay, ≠Ø - 3 minutes delay)

$D_BD_CD_D$ - number of tests done K (Ø - 999)

$D_ED_FD_{10}$ - number of breakdown B (Ø - 999)

$D_{11}D_{12}D_{13}$ - number of non-breakdown NB (Ø - 999).

This arrangement of specifications provides flexibility of including identifiers and saving in program memory. All specifications are typed in one line terminating by 'carriage return'. It should be noted that all input/output numbers

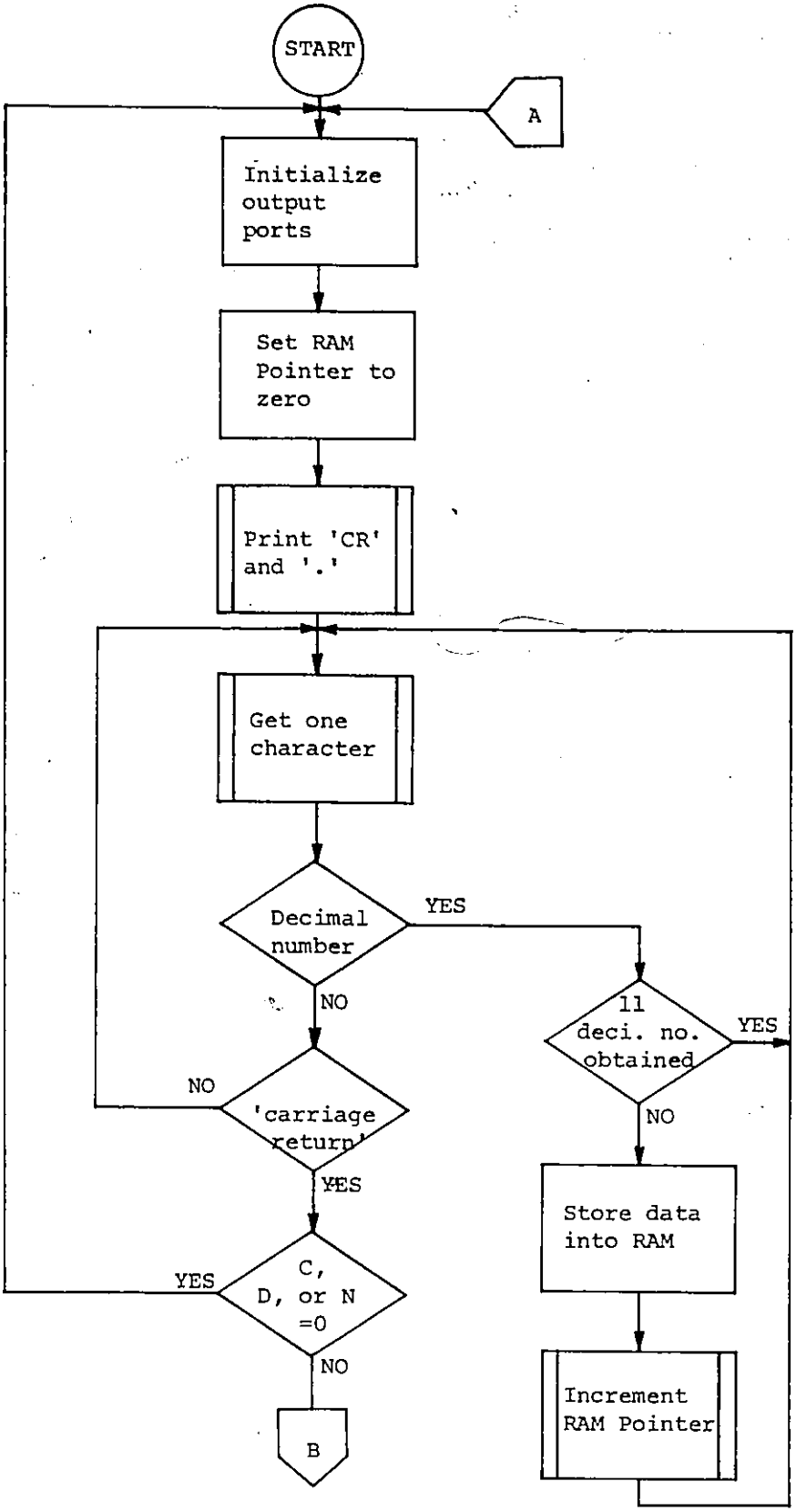


Figure 9. The flow chart of firmware mainline

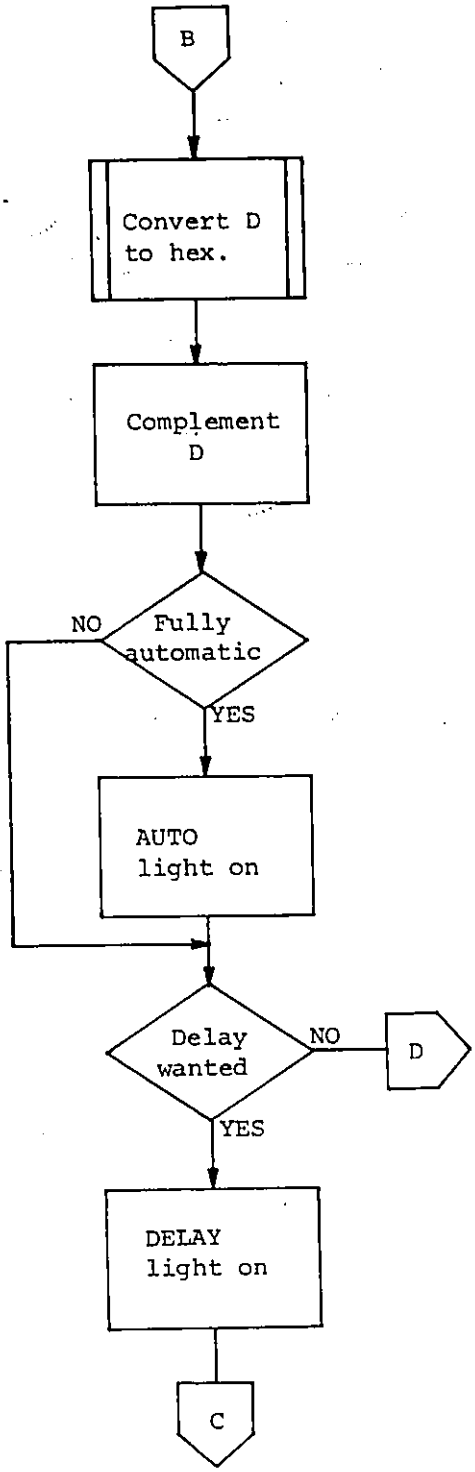


Figure 9 . (Cont.)

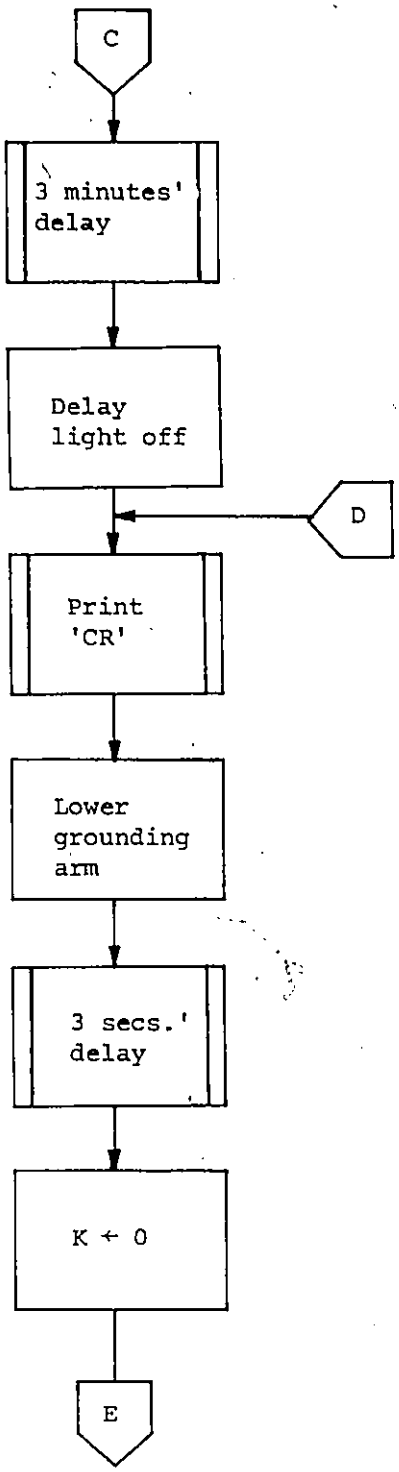


Figure 9 . (Cont.)

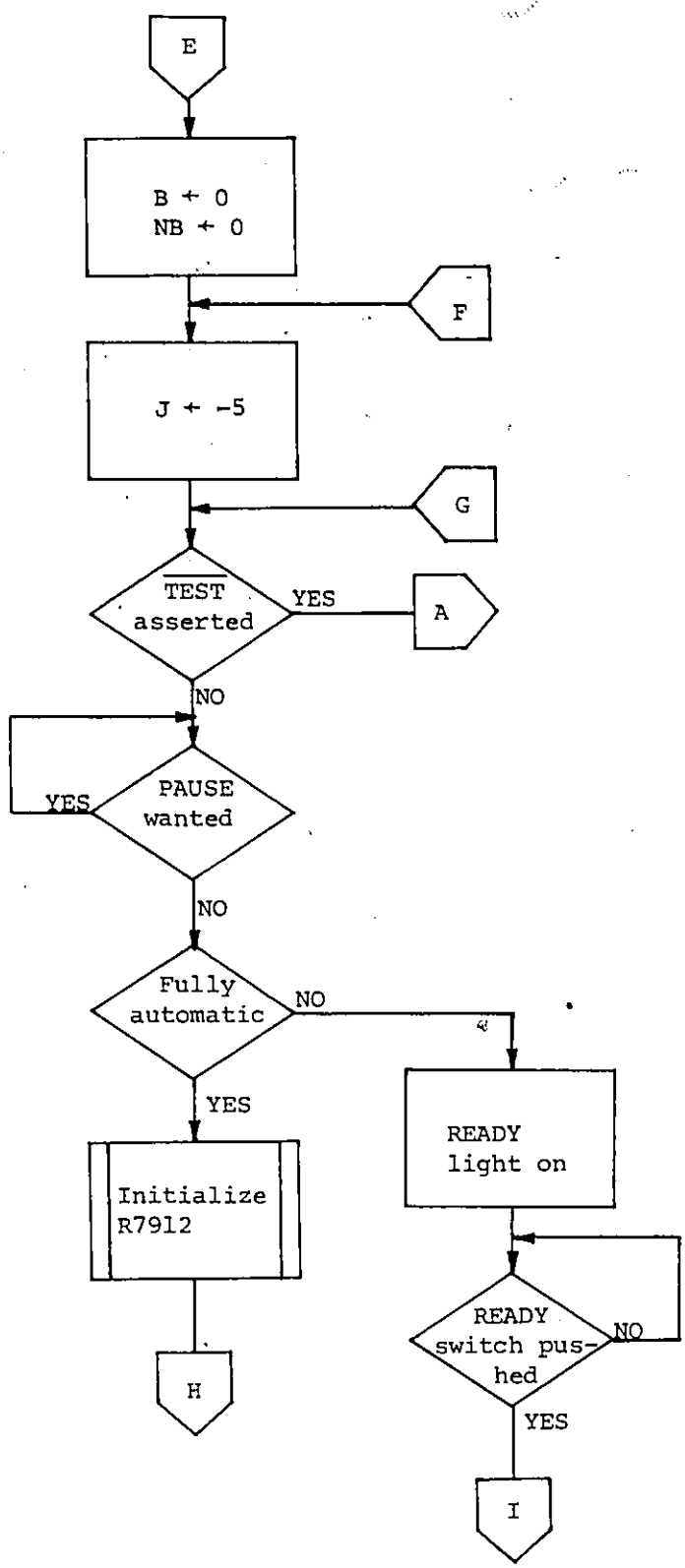


Figure 9. (Cont.)

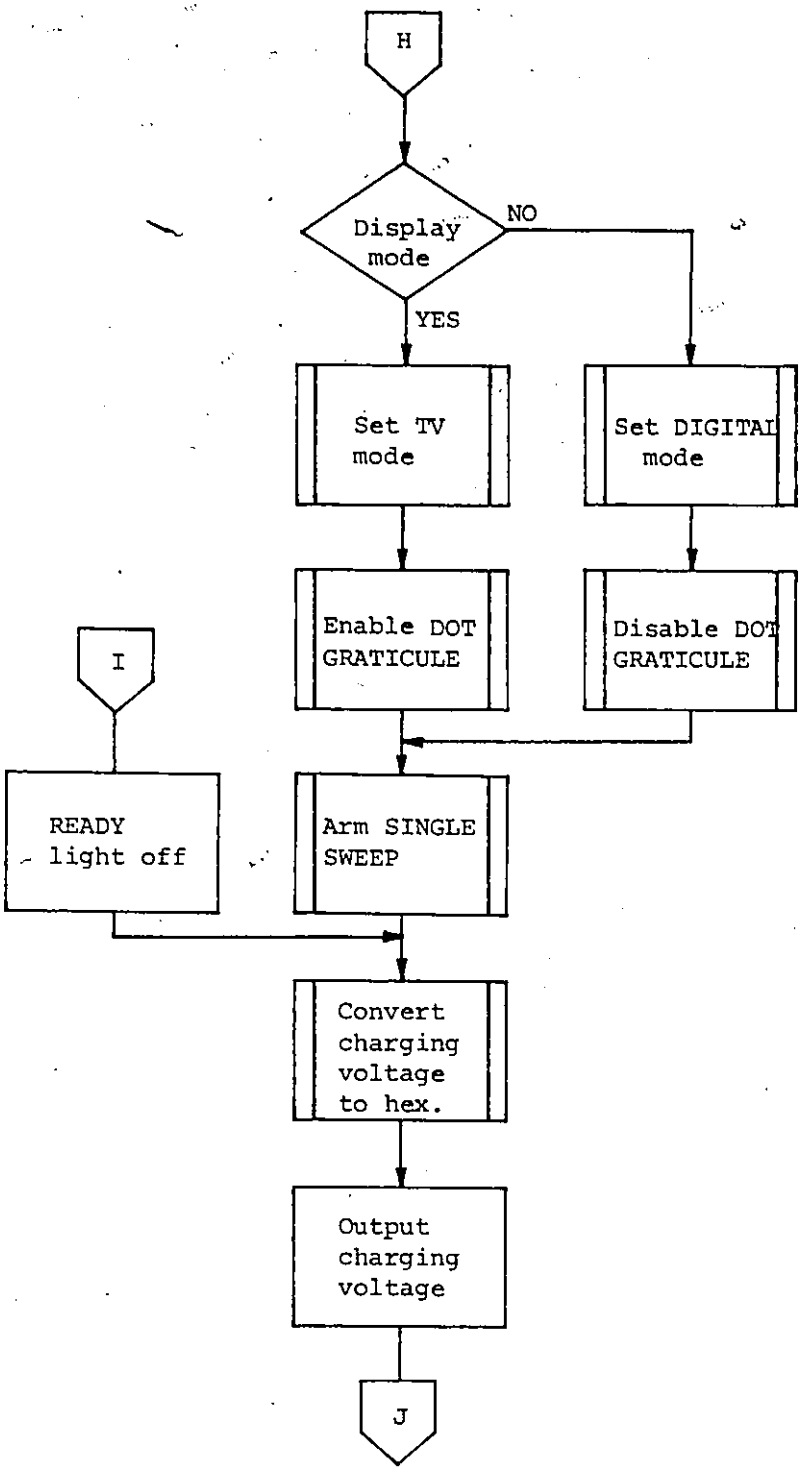


Figure 9 . (Cont.)

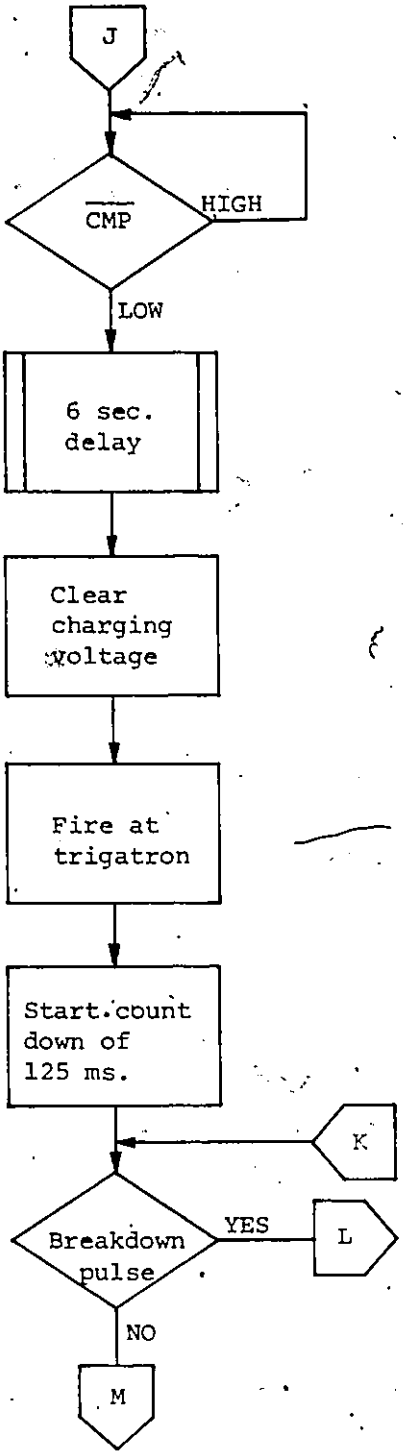


Figure 9 . (Cont.)

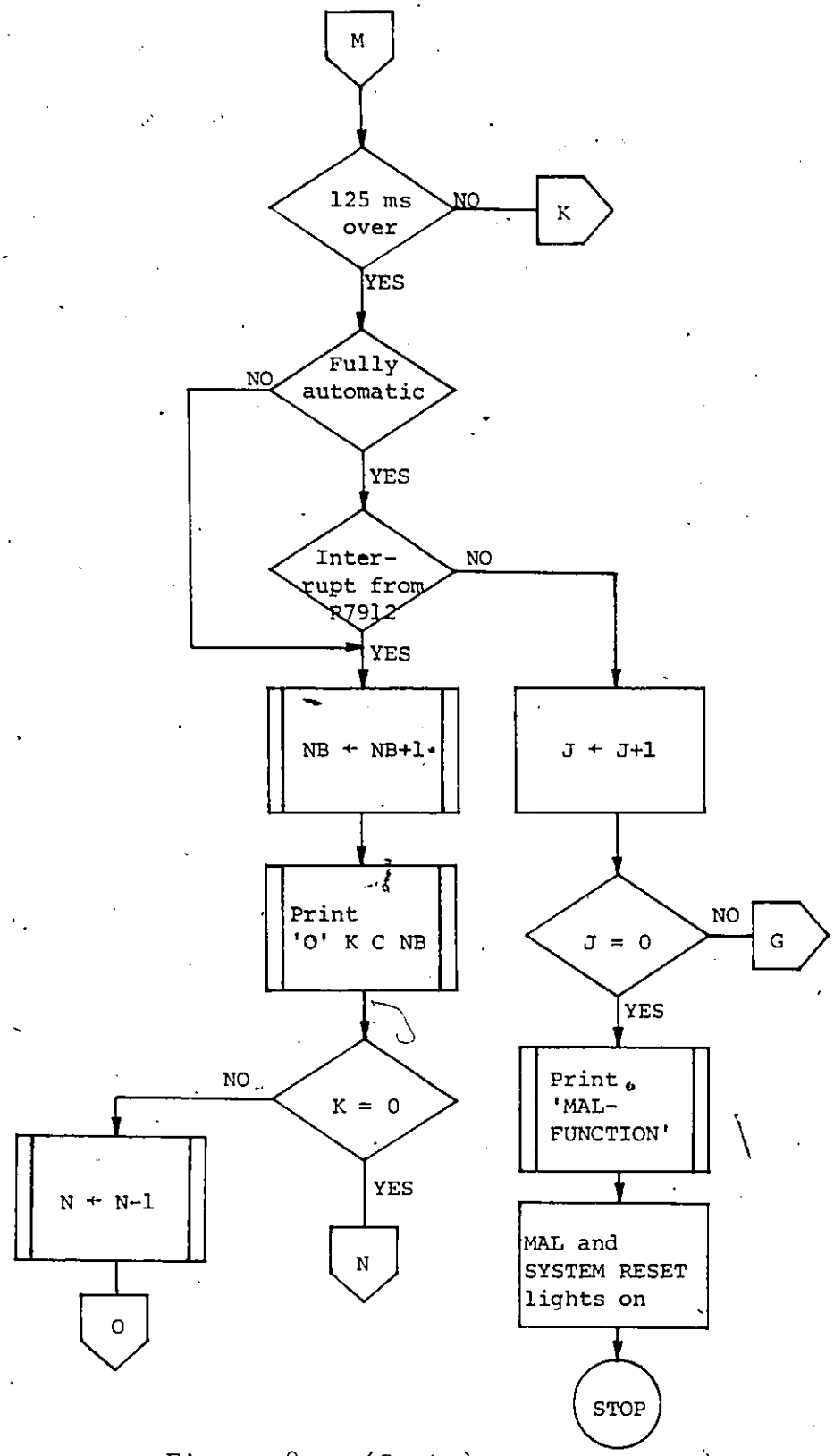


Figure 9 . (Cont.)

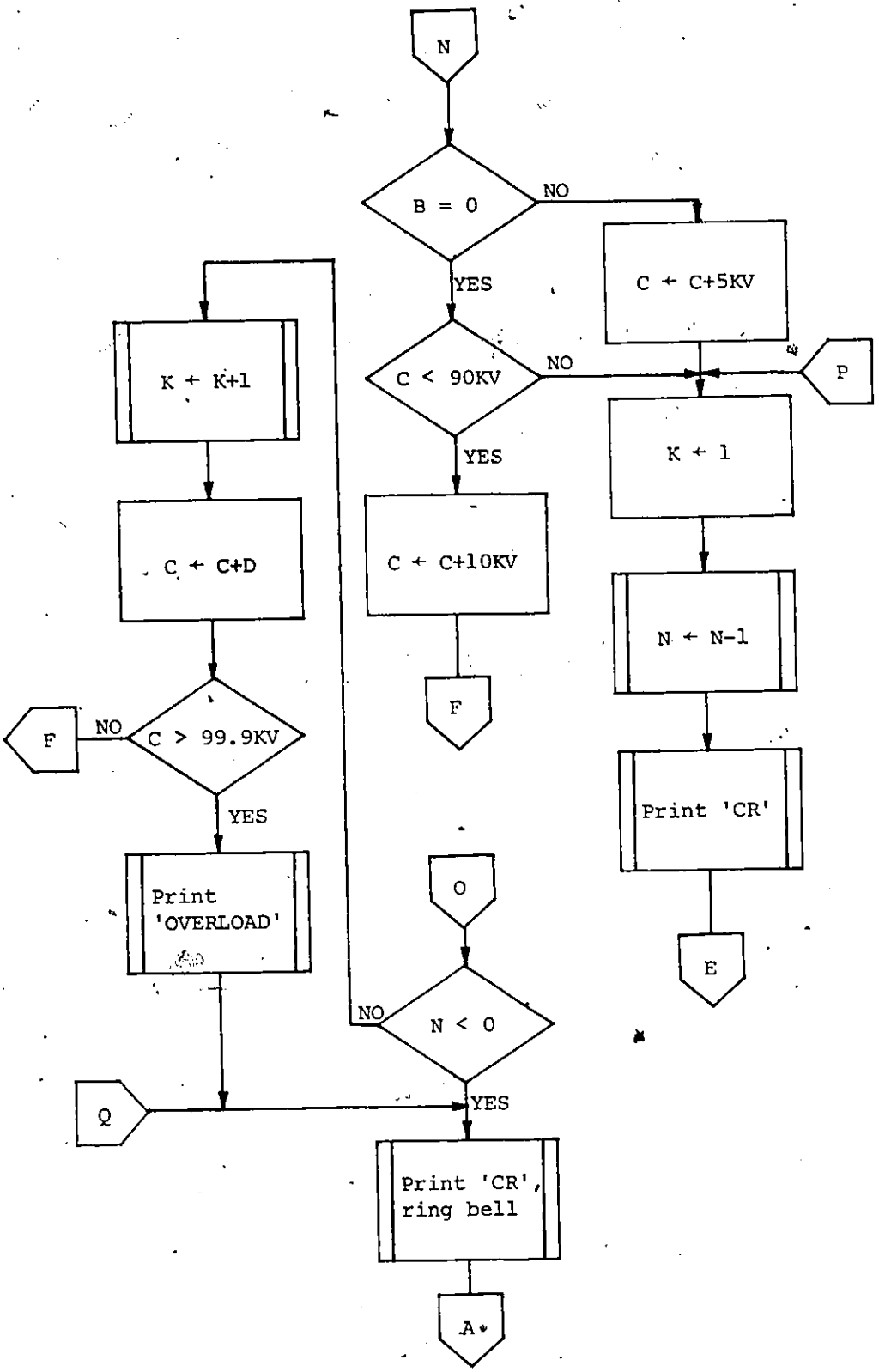


Figure 9 . (Cont.)

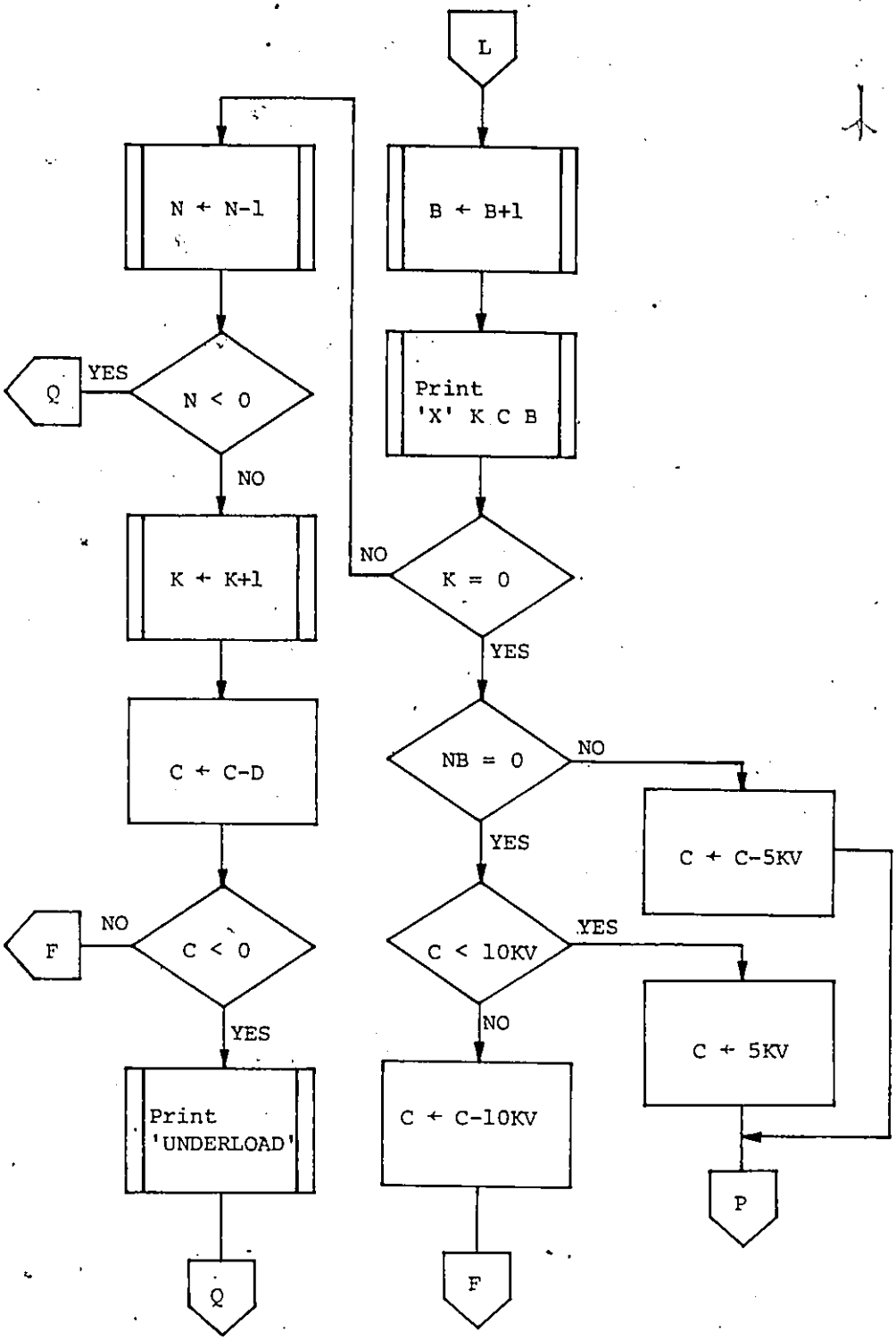


Figure 9 . (Cont.)

through the Teletype are in decimal, but some of them, such as charging voltage and incremental voltage, are converted internally to hexidecimal for programming purposes. Validity of specifications is checked. If any one of the charging voltage, incremental voltage or sample size is zero, program pointer is set to zero and program restarts.

When the system is operated fully automatically, the AUTO light is on. 3 minutes' delay of testing gives an operator time to leave the laboratory before testing starts, if so desired. This option should only be used in fully automatic mode. The grounding arm is a safety feature for the impulse generator. It is used to ascertain discharge of the capacitors. Thus it is lowered before charging the impulse generator. Counters such as B and NB are initialized to zero before testing. Register #4 is used as counter for malfunction. In fully automatic operation malfunction of the system can be detected by the response of the transient digitizer after the trigatron is fired. If no signal is received, $\overline{\text{CB}}\text{ØØ}$ will not be asserted. When this happens, that particular test is ignored and tried again. If this condition persists for five consecutive trials, error message "MALFUNCTION" is printed out, MAL light is on and program counter is reset. Since there is no interrupt facility in 4ØØ4, routine scanning of the states of TEST RESET, PAUSE and TV switches is necessary and the program branches to appropriate routine accordingly. READY switch is used in

semi-automatic operation only. After it is lighted, testing activity will resume and READY light will be off if READY switch is pushed. Features of the transient digitizer can be controlled manually or by commands sent from the CPU on $\overline{CB00}$ - $\overline{CB12}$ lines. Some of the commands executed are (in octal with $\overline{CB00}$ being the least significant bit):

4000 - initialize R7912

2005 - select TV mode

2014 - enable dot graticule

2015 - select digital mode

2004 - disable dot graticule

2040 - arm single sweep.

Charging voltage is stored in decimal form. It is converted to hexidecimal for output to the 10-bit D/A converter. When the impulse generator is charged up, the comparator output $\overline{CMP}$ from the control unit drops from 5 V to 0 V and 6 seconds' delay is required before firing. Then the CPU checks for the presence of a breakdown pulse within 125 millisecond. After 125 millisecond, if there is no malfunction and no breakdown, the counter NB is incremented by 1 and result is printed on the Teletype in the form of

O K C NB

where "O" indicates no breakdown. At the same time they are also punched on paper tape for data analysis. As described earlier, a rough search of the mean is carried out before the actual testing. This search is distinguished by the value of K being zero. When a mean is established, K is then set to

1 and actual testing using the "up-and-down" method begins. During the course of testing, charging voltage C and counters such as M, K, B and NB are adjusted accordingly. If a breakdown pulse is detected within 125 millisecond, the procedure described in section 4.4.a. is performed and appropriate counters are adjusted. The result printed is in the form of

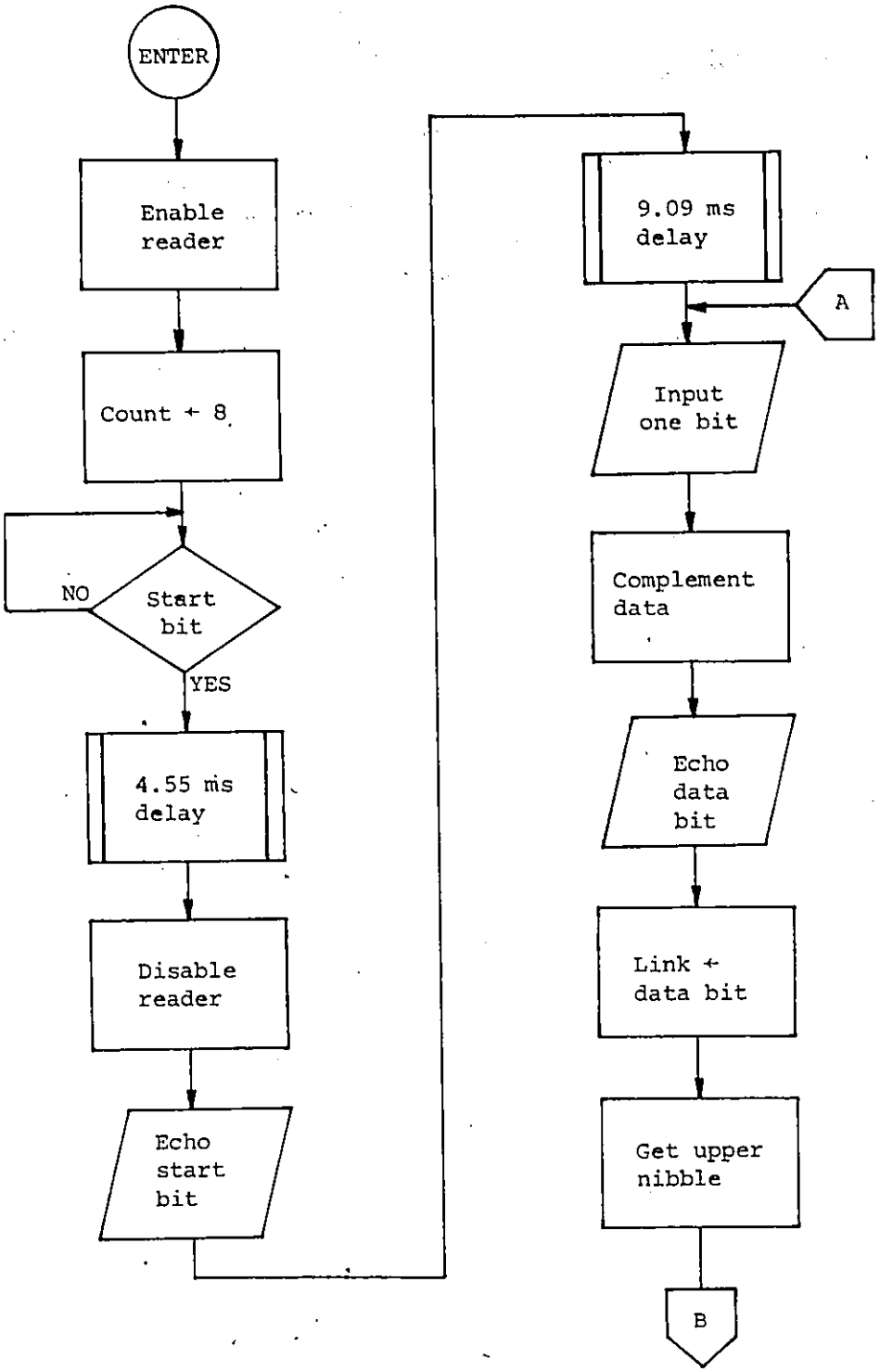
X K C B

where "X" indicates breakdown. While testing if charging voltage is over 99.9 KV, "OVERLOAD" will be printed out and if it is under 0 KV, "UNDERLOAD" will be printed out and program counter is reset. At the end of testing "&" is printed out and the bell is rung.

4.3.c. THE SUBROUTINES

The programs are commented in great detail as can be seen in Appendix A. Flow charts of the major subroutines are presented in Figure 10 to 12. The input/output subprograms of peripherals such as the Teletype and the transient digitizer are written according to their requirements and are self-explanatory.

Conversion of a 3-digit binary coded decimal number (BCD) to hexidecimal shown in Figure 13 is performed by repeatedly subtracting 16_{10} from the number and adjusting the appropriate hexidecimal digits until that number is less than 16_{10}. Then this number is set as the least significant digit of its hexidecimal representation. BCD subtraction of 2-digit



(a). Input one character from Teletype

Figure 10. Teletype input/output routines

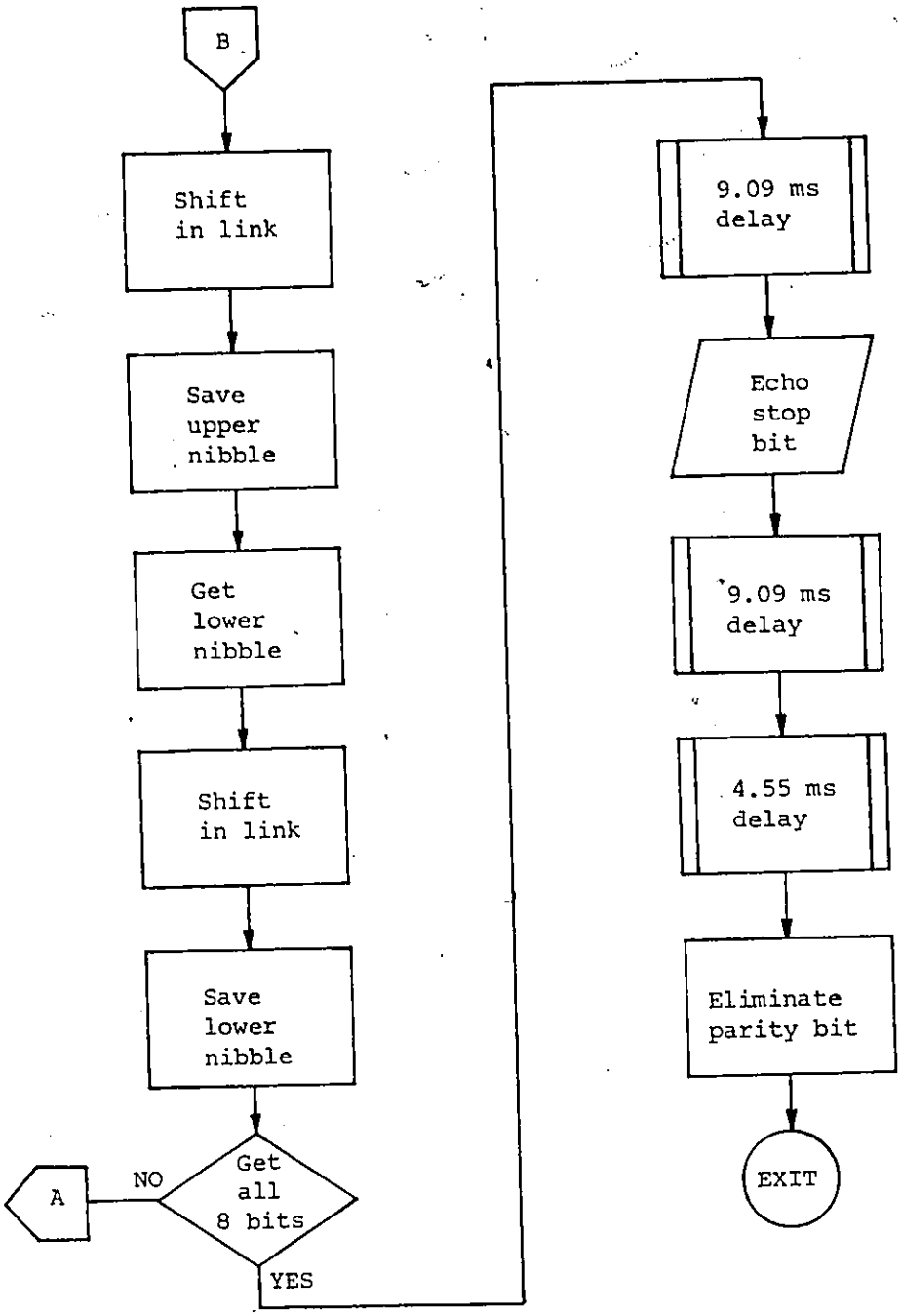
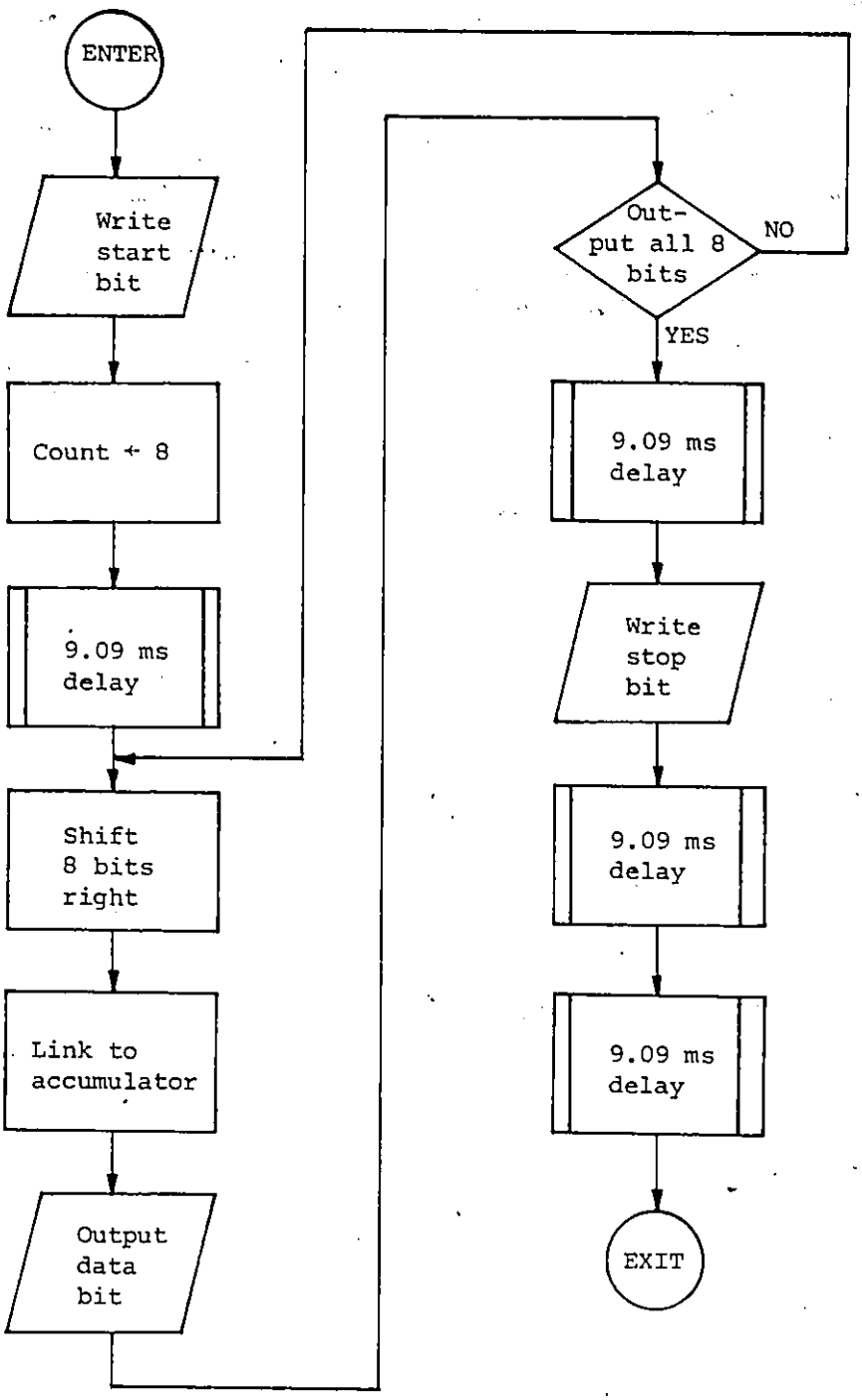


Figure 10. (Cont.)



(b). Output one character to Teletype

Figure 10. (Cont.)

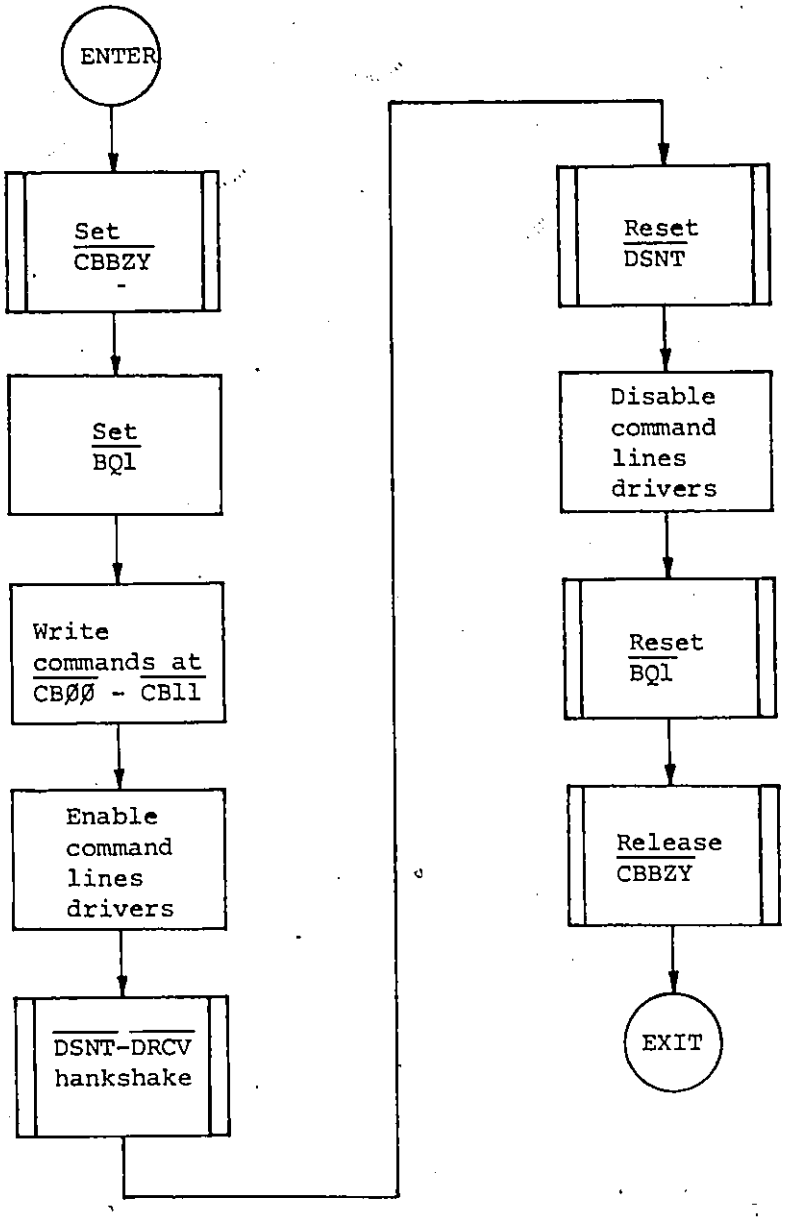
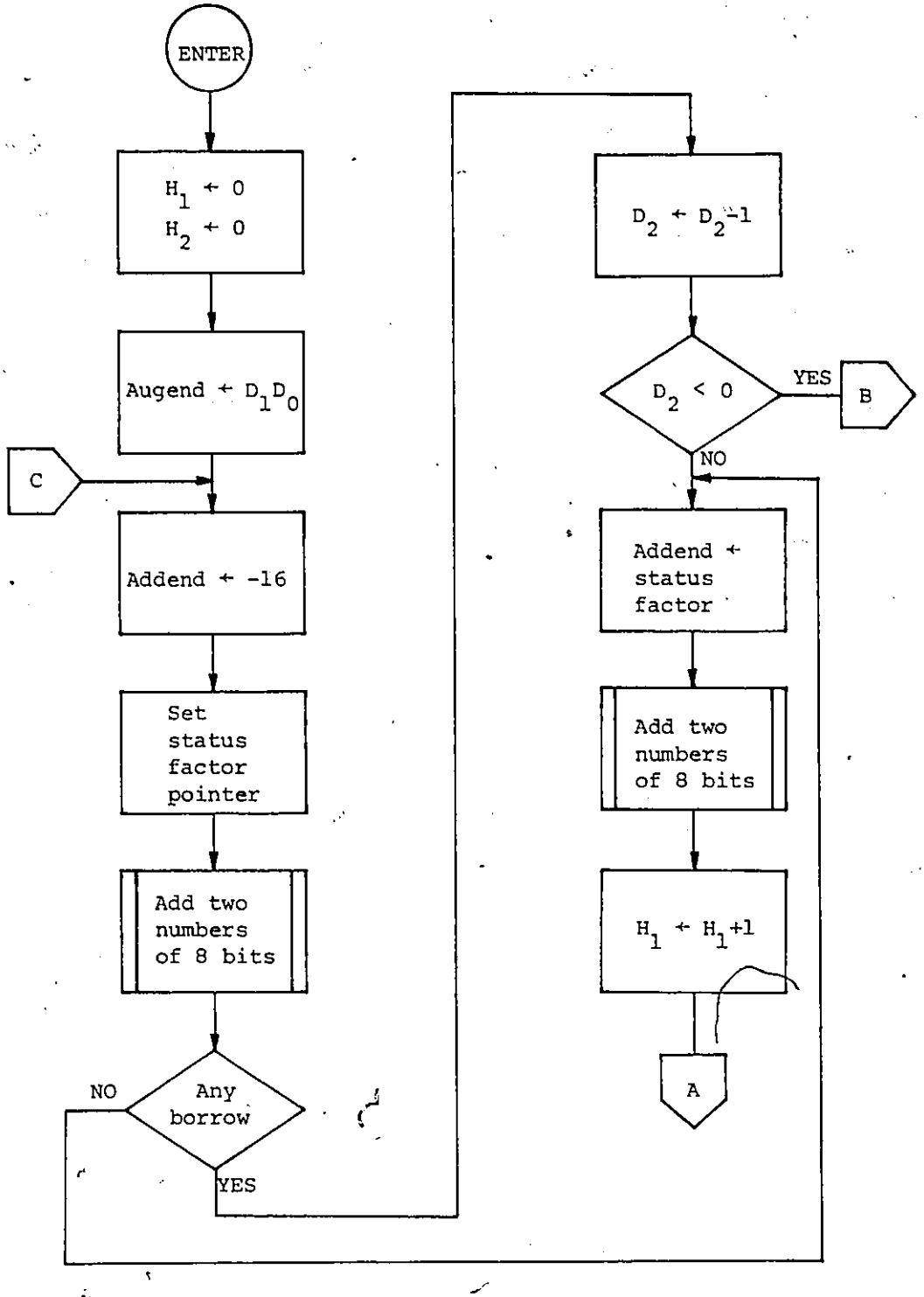


Figure 11. R7912 Transient Digitizer command routine



(a) Convert a 3-digit BCD number to hexadecimal

Figure 12. Conversion from decimal to hexadecimal routines

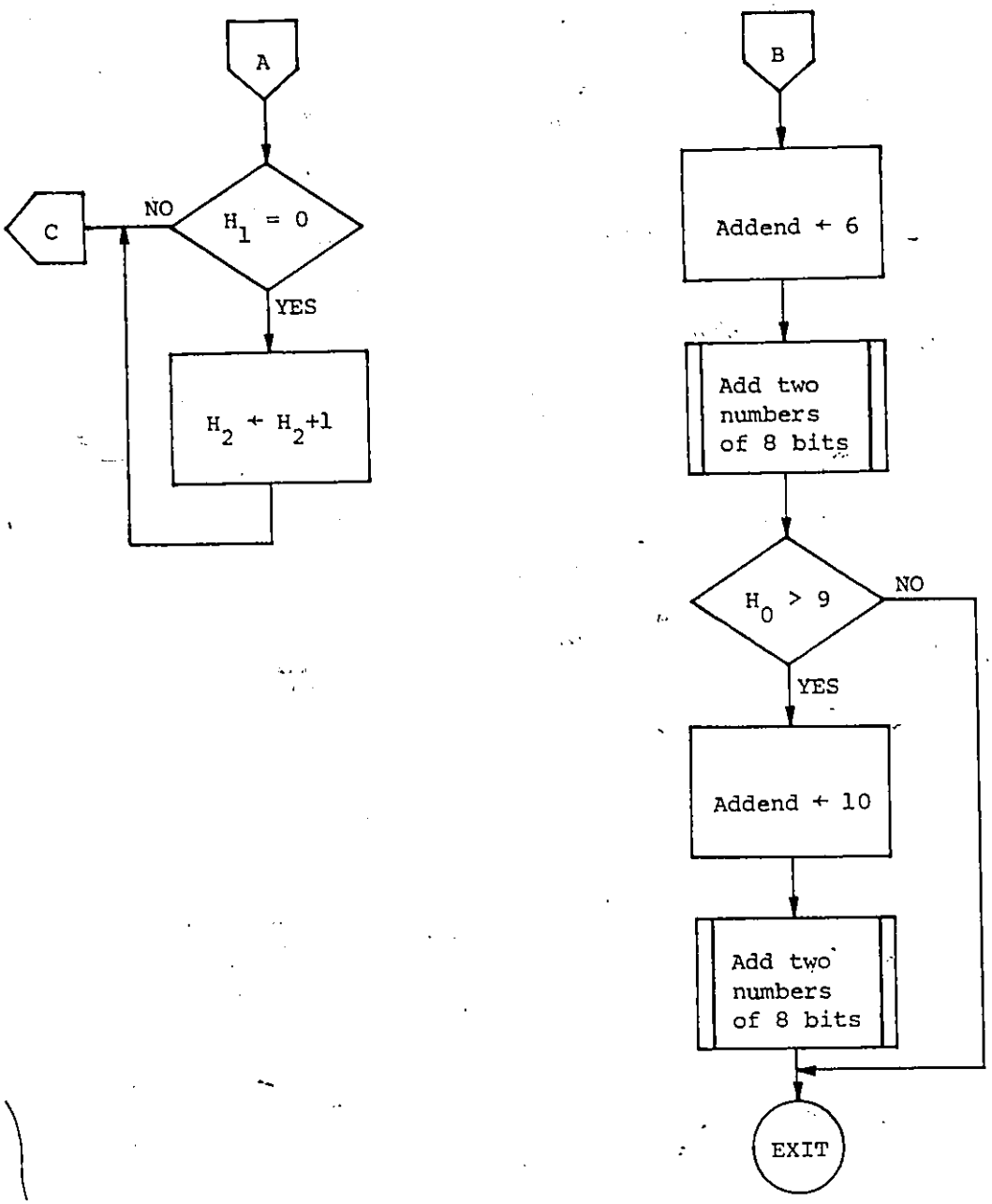
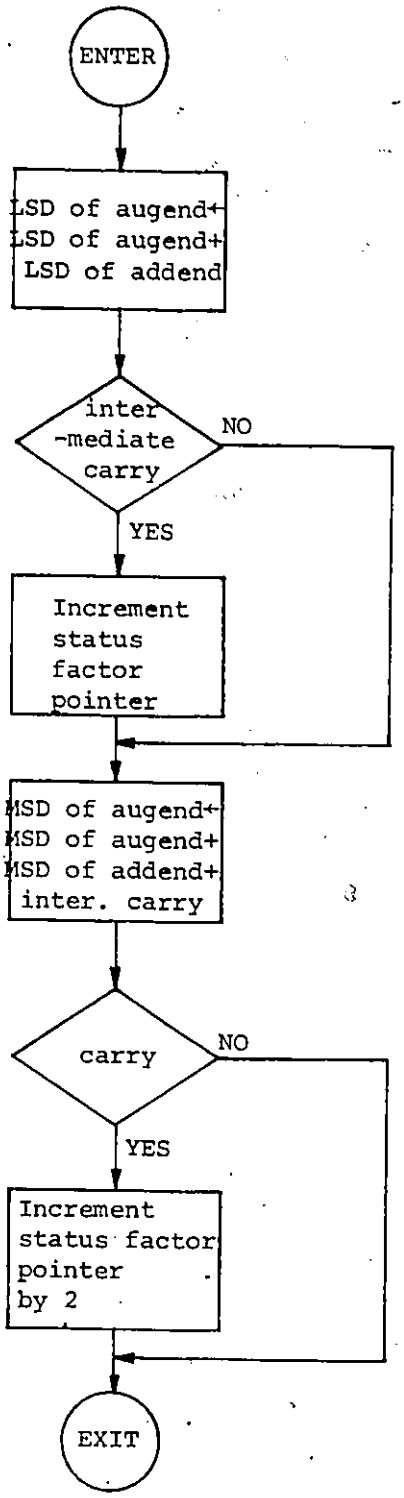


Figure 12. (Cont.)



(b). Add two numbers of 8 bits

Figure 12. (Cont.)

numbers is done by adding the two's complement of the subtrahend (here 16_{10}) to the minuend (the two lower order digits of the number being converted). The carry generated in this step reflects the true carry to the next higher digit. Then a factor is added to this sum using binary addition. The factor to be added depends on the carry and intermediate carry as follows:

C	IC	FACTOR
Ø	Ø	$9A_{16}$
Ø	1	$AØ_{16}$
1	1	FA_{16}
1	1	$ØØ_{16}$

The mainline program and its subprograms discussed in this chapter are presented in Appendix A. Due to the limited size of program memory, the programs are written in its most optimal arrangement.

4.4. CONTROL AND DISPLAY PANEL

The control and display panel of Figure 13 together with a Teletype are the operator's interface to the CPU. Its features are summarized in this section.

After the system is initialized and specifications are loaded through the Teletype, AUTO is on if the system is operated fully automatically and off it is operated semi-automatically. Once chosen this operation remains unchanged throughout testing. If delay option is indicated, DELAY is on for 3 minutes and then off. Testing starts after this time

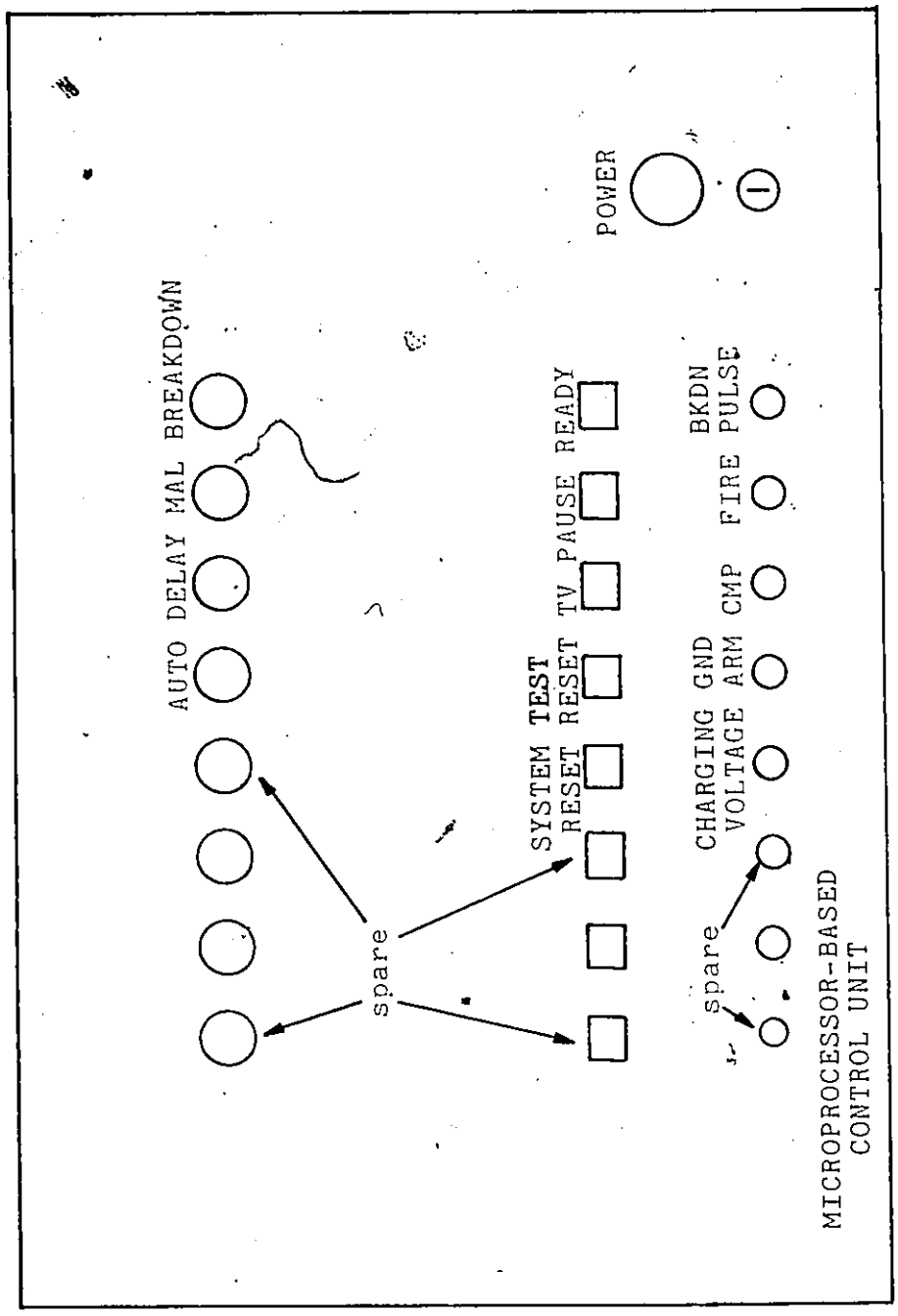


Figure 13. Control and display panel

lag. In fully automatic operation if after five consecutive trials without any response from the transient digitizer, MAL is on and program restarts. This indicates no signal is received by the digitizer and possible disconnection is present in the system. The operator should locate the cause and correct it before doing another set of testing. If flashover occurs in a test, BREAKDOWN is on and off, otherwise.

When SYSTEM RESET is pushed, the CPU is reset and RAMs are cleared. It requires .35 millisecond to clear all the RAMs, the action of push and release the switch usually provides more than enough time. After the generator is charged, TEST RESET should be used if the operator wishes to reset the system. This ensures discharging of impulse generator before resetting. The display/digital mode of the transient digitizer can be changed by pushing the TV switch. When TV switch is lighted, the display mode is chosen, otherwise the digital mode is selected. The PAUSE switch is used usually in fully automatic operation for temporary stopping the test before charging the generator. It is lighted when initially pushed. The program pointer then enters an idle loop just before charging of the generator, and program continues and the light is off after it is pushed again. In semi-automatic operation, it is necessary to push the READY switch after it is illuminated for continuation of testing.

Besides the two connectors at the back of the chassis for the Teletype and the transient digitizer, five BNC

connectors are provided for signals to and from the control unit. All signals except CHARGING are of TTL levels. At CHARGING an analog signal within 0 - 5 V corresponding to 0 - 100 KV is provided. Setting high level on GND ARM lowers the grounding arm and low level raises it. Through a comparator on the control unit the preset charging level is compared to the voltage level of the generator. When they are different the output of the comparator $\overline{CMP}$ is high. $\overline{CMP}$ drops to low when the generator is charged up to the preset charging level. Then after 6 seconds a FIRE pulse triggers the spark gap. After firing, if BDP pulse is received within 125 millisecond, flashover is indicated.

Two power supplies are used to provide DC power to the system. The +5 V, -10 V supply is fused with a 3 A slow-blow fuse and the ±15 V supply is fused with a 1.5 A slow-blow fuse. Each DC output has individual overvoltage protection. The DC outputs are bounded within +5%. When the source voltage rises above the preset threshold level, the SCR on the overvoltage protection circuit is triggered on causing what appears to be a short across the DC source, thereby reducing the DC source voltage to near zero and protecting the integrated circuits from being damaged. The overvoltage protection will recover or reset automatically when the power supply is turned off and the capacitors have discharged.

4.5. ANALYSIS SOFTWARE

A general purpose minicomputer system (NOVA 840) is used to analyse the data obtained from the method of section 4.3. because considerable memory is required for statistical analysis. A punched paper tape of data is prepared while the test is running. This data is then analyzed using formulas of the "up-and-down" method.

4.5.a. STATISTICAL ANALYSIS OF THE "UP-AND-DOWN" METHOD

The statistical analysis of data obtained by using the "up-and-down" method can be quite simple provided that the experiment satisfies certain conditions. While the "up-and-down" method is particularly effective for estimating the mean, it is not a good method for estimating small or large percentage points unless normality of the distribution throughout a wide range is assured. A further condition is that the standard deviation of the normally distributed variate must be estimated roughly in advance. The interval between testing levels should be approximately equal to the standard deviation. This condition is not severe, since it will be well enough satisfied if the interval actually used is less than twice the standard deviation. The operator should be well awared of these conditions such that the experiment is carried out within the accuracy of this method.

The analysis involves only the symbol occurring less frequently. If y_0 is the lowest level of this symbol, the

data can be arranged by letting $y_i = y_o + iD$ and the frequency of occurrence at the level y_i be n_i. The sums N, A and B of n_i, in_i and i^2n_i are then obtained respectively. The estimates of the statistical parameters of interest are given as follows:

Estimate of mean μ : $\bar{y} = y_o + D(A/N \pm 1/2)$ (4.1) [2]

(+ if based on symbol at lowest level,

- if based on symbol at highest level).

Estimate of standard deviation σ :

$S = 1.620D\{(NB - A^2)/N^2 + 0.029\}$ (4.2) [2]

(valid only if $(NB - A^2)/N^2 > .3$)

Estimate of 100p% point $\mu + Z_p\sigma$: $\bar{y} + Z_pS$ (4.3) [2]

(Z_p is the Z for $F(Z) = p$ in the Normal Distribution Table)

Estimate of standard deviation of $\bar{y}$:

$S_{\bar{y}} = (6S + D)/(7\sqrt{N})$ (4.4) [2]

(valid only if $D < 3\sigma$)

Estimate of standard deviation of S :

$S_s = (1.1S + 0.3S^2/D)/\sqrt{N}$ (4.5) [2]

(valid only if $D < 2\sigma$)

Estimate of standard deviation of $\bar{y} + Z_pS$:

$S_{\bar{y}+z_ps} = \sqrt{(S_{\bar{y}}^2 + Z_p^2S_s^2)}$ (4.6) [2]

Approximate $100(1 - \alpha)\%$ confidence limits for any parameter are obtained by taking its estimate and adding and subtracting $t_{\alpha/2,N-1}$ times the estimate of its standard deviation.

The general formulas shown above can also be used to determine sample size. If an estimate of standard deviation

S_σ is made from previous experience, this estimate should be substituted for S in the formula shown above for $S_{\bar{y}}$, S_s or $S_{\bar{y}+z_p s}$ in order to determine the sample size required for a prescribed precision for a chosen parameter. To determine a parameter within tolerance of ±T with $100(1 - \alpha)\%$ confidence, that parameter must not be greater than $T/t_{\alpha/2,N-1}$. The new sample size is at least twice the N obtained from one of the following formulas:

$$\text{for } \mu : N > \{(6S_\sigma + d)t_{\alpha/2,N-1}/(7T)\}^2 \qquad (4.7) \quad [2]$$

$$\text{for } \sigma : N > \{(1.1S_\sigma + .3S_\sigma^2/d)t_{\alpha/2,N-1}/T\}^2 \qquad (4.8) \quad [2]$$

$$\text{for 100p\% point} : N > \{(6S_\sigma + d)^2/7^2 + Z_p^2 \cdot (1.1S_\sigma + .3S_\sigma^2/d)^2\}(t_{\alpha/2,N-1}/T)^2 \qquad (4.9) \quad [2]$$

where d is the new increment and could be taken as $1.5\ S_\sigma$.

4.5.b. THE ALGORITHM

The analysis program of Appendix B is written in FORTRAN 5 language. Its algorithm of Figure 14 is very simple. Values of D, p, α, T, S_σ and d are accepted from the console keyboard. The data on paper tape is fed in through the Teletype tape reader and then analyzed using the formulas of last section. The data of symbol occurring less frequently is then rearranged and manipulated as described in last section. All quantities mentioned earlier are calculated. The complete analysis is printed out on the line printer.

4.6. SYSTEM IMPLEMENTATION

Complete testing procedure includes setting up of

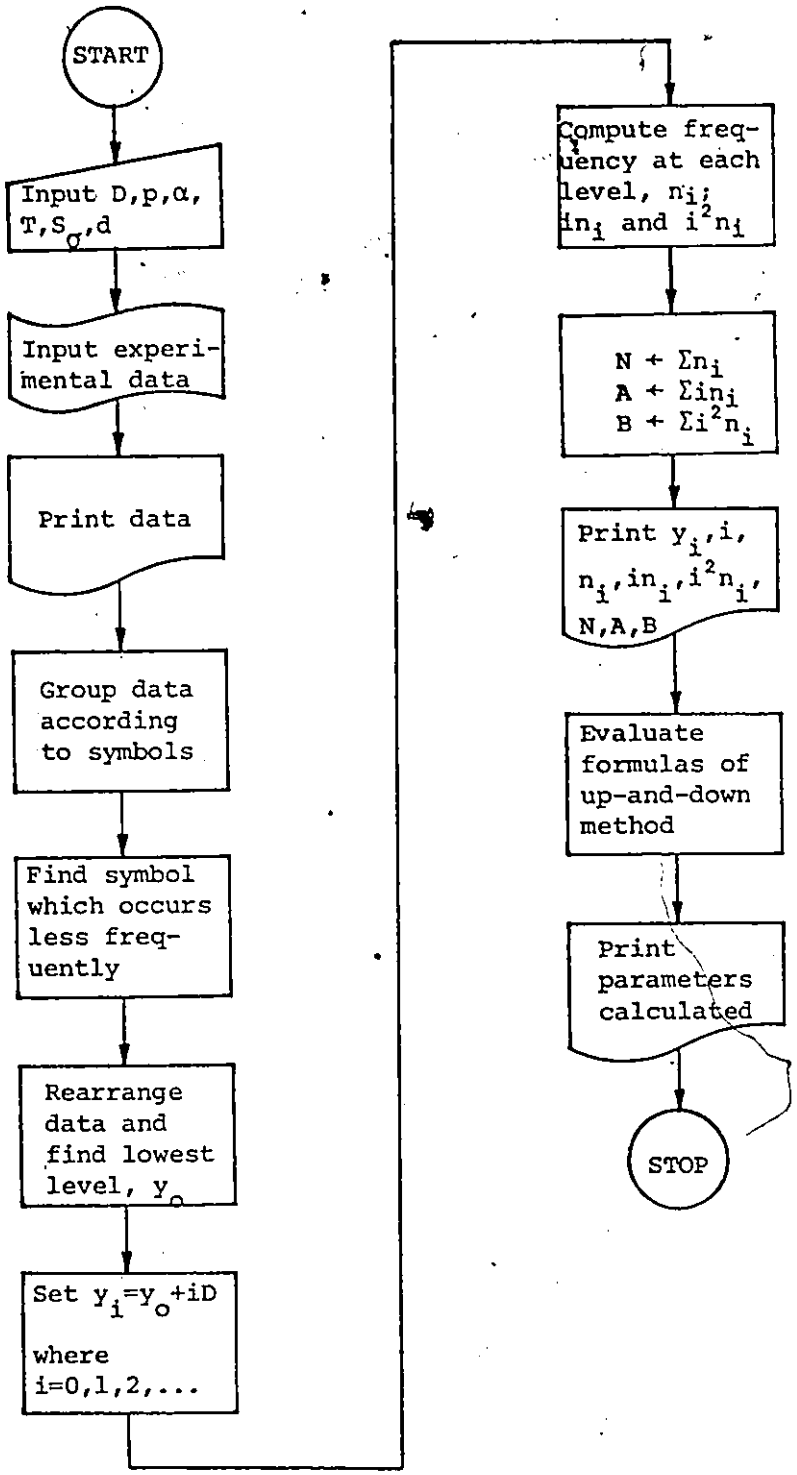


Figure 14. The flow chart of analysis software

equipments, operating the system and analyzing the data. In the set-up mode, the operator chooses to operate the system manually, semi-automatically or fully automatically and connects up the equipments as described in Chapter 2. After having initialized the system, the transient digitizer is set as follows:

READOUT - OFF

GRATICULE - ON

MODE - NON-STORE

TIME BASE - SINGLE SWEEP.

The control unit is then switched to automatic. The specifications are loaded through the Teletype. The operation mode has been discussed in great detail in previous chapters and will not be repeated here.

At the completion of testing, data punched on paper tape is obtained. In the analytical mode, content of this tape is loaded in the NOVA Real-Time-Disc Operating System. Data is then analyzed with print-out of the statistical analysis. To achieve this, the following steps are carried out in proper sequence. Response from the computer is underlined.

1. Power up NOVA RDOS; load in disk and push RUN; when amber light comes on toggle RESET and PROGRAM LOAD switches.
2. Power up line printer and push SELECT.
3. Load paper tape in tape reader; set Teletype to LINE and paper tape reader to START.

4. Select LOCAL on the Tektronix Display Unit.

5. Through the console keyboard type in proper commands. Here is an example.

```
FILENAME ? SYSØØØ↓
DATE(M/D/Y) ? 5 16 77↓
TIME(H:M:S) ? 9 45 5↓
R
DIR DP1↓
R
DIR INTEL↓
R
UPDOWN↓
TURN ON TAPE READER AND LINE PRINTER
INCREMENTAL VOLTAGE D (IN KV) = 1Ø.Ø↓
CUMULATIVE DISTRIBUTION FUNCTION P = .1↓
LEVEL OF SIGNIFICANCE, ALPHA = .Ø5↓
FOR DETERMINING NEW SAMPLE SIZES:
TOLERANCE = 5.Ø↓
ESTIMATE OF STANDARD DEVIATION = 1Ø.Ø↓
NEW INCREMENT, D(NEW) (IN KV) = 15.Ø↓
LOAD $TTRI, STRIKE ANY KEY
↓

STOP
R
```

↓ stands for 'carriage return'. The complete analysis is printed on the line printer. Additional analysis is performed if the tape is reloaded, UPDOWN and specifications

are typed again.

6. When finished, type

RELEASE INTEL↓

R

RELEASE DP1↓

R

RELEASE DPØ↓

MASTER DEVICE RELEASED

Push LOAD; when white light comes on, unload the disk and turn off power for all devices.

CHAPTER FIVE

TESTING

5.1. PHASES OF TESTING

Testing of the microprocessor-based controller falls into three phases: primary, intermediate and final.

The primary phase was carried out utilizing the MCS-4 development system. The control software was loaded in RAM of the MCS-4 and was executed. Predetermined execution paths were checked out by using the pass count and latching feature provided at the display and control panel of the MCS-4. Most of the software bugs were then removed.

Since some of the lines from the processor module IMM4-42, such as $\overline{IN}$, $\overline{OUT}$, CØ-3, and I/O bus, were not available at the ports of the MCS-4, more complete debugging of the hardware required interfacing the processor module and the interface board. The intermediate phase included bread-boarding the interface module and executing the firmware in PROM. At this stage the remaining software bugs and all of the hardware bugs were taken out. The hardware design was further refined to eliminate physical problems such as bouncing effect of switches. The system was well defined upon completion of this phase.

The physical layout of the unit and a printed-circuit board were then designed. The unit was constructed and the printed-circuit board was assembled. Wire-wrap connector blocks were used and all IC's were housed in sockets for

ease of debugging and maintenance.

The final phase was performed by integrating the control and display panel, the interface module, the processor module and the firmware to carry out testing under all possible conditions. This stage was mainly provided for debugging the printed-circuit board and wiring. After this phase a unit meeting all the requirements specified was produced and ready to be operated in any of the system configurations as described in section 2.3.

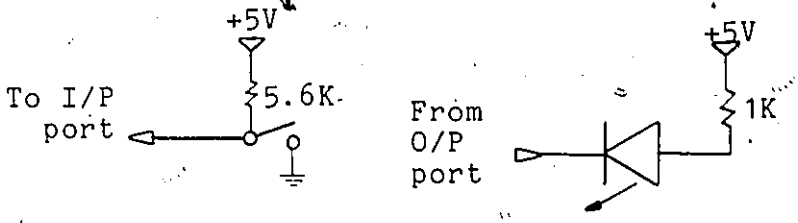
5.2. SIMULATION

Due to circumstances that an element of the test system, namely the control unit which was the responsibility of other individual, was not yet completed, system integration could not be performed. The final testing was thus accomplished by simulation.

A simulation board was then constructed. Charging voltage which was a DC level between ØV and 5V with resolution of 5mV was displayed on an oscilloscope. The other I/O signals from the microprocessor-based control unit were TTL compatible. Thus as shown in figure 15 LED's were used to display output states and switches with pull-up resistors were used to set input states. Layout of the simulation board is illustrated in figure 16.

All possible conditions listed as the following are imposed and tested:

For unidirectional bus:



For bidirectional bus:

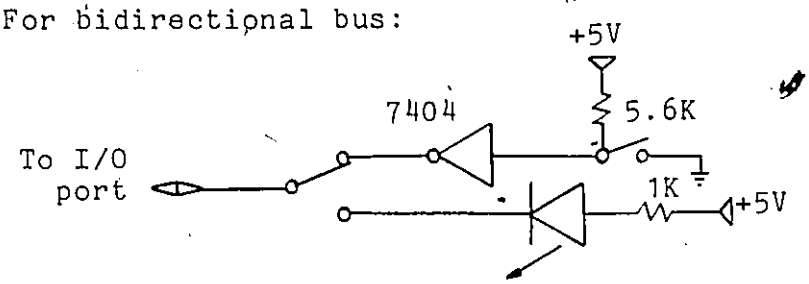


Figure 15. Driving circuit for simulation

1. $M = \emptyset$
2. $D = \emptyset$
3. $C = \emptyset$
4. With delay (DELAY $\neq \emptyset$)
5. Without delay (DELAY $= \emptyset$)
6. Semi-automatic operation (AUTO $= \emptyset$)
7. Fully automatic operation (AUTO $\neq \emptyset$)
8. Starting voltages under the following conditions:

   i. $C_1 = C_{last} - 5.\emptyset$ KV

   for NBD ... NBD BD where $1\emptyset.\emptyset$ KV $< C_{last} < 9\emptyset.\emptyset$ KV

   ii. $C_1 = C_{last} + 5.\emptyset$ KV

   for BD ... BD NBD where $1\emptyset.\emptyset$ KV $< C_{last} < 9\emptyset.\emptyset$ KV

   iii. $C_1 = C_{last}$

   for NBD ... NBD where $C_{last} > 9\emptyset.\emptyset$ KV

   iv. $C_1 = 5.\emptyset$ KV

   for BD ...BD where $C_{last} < 1\emptyset.\emptyset$ KV

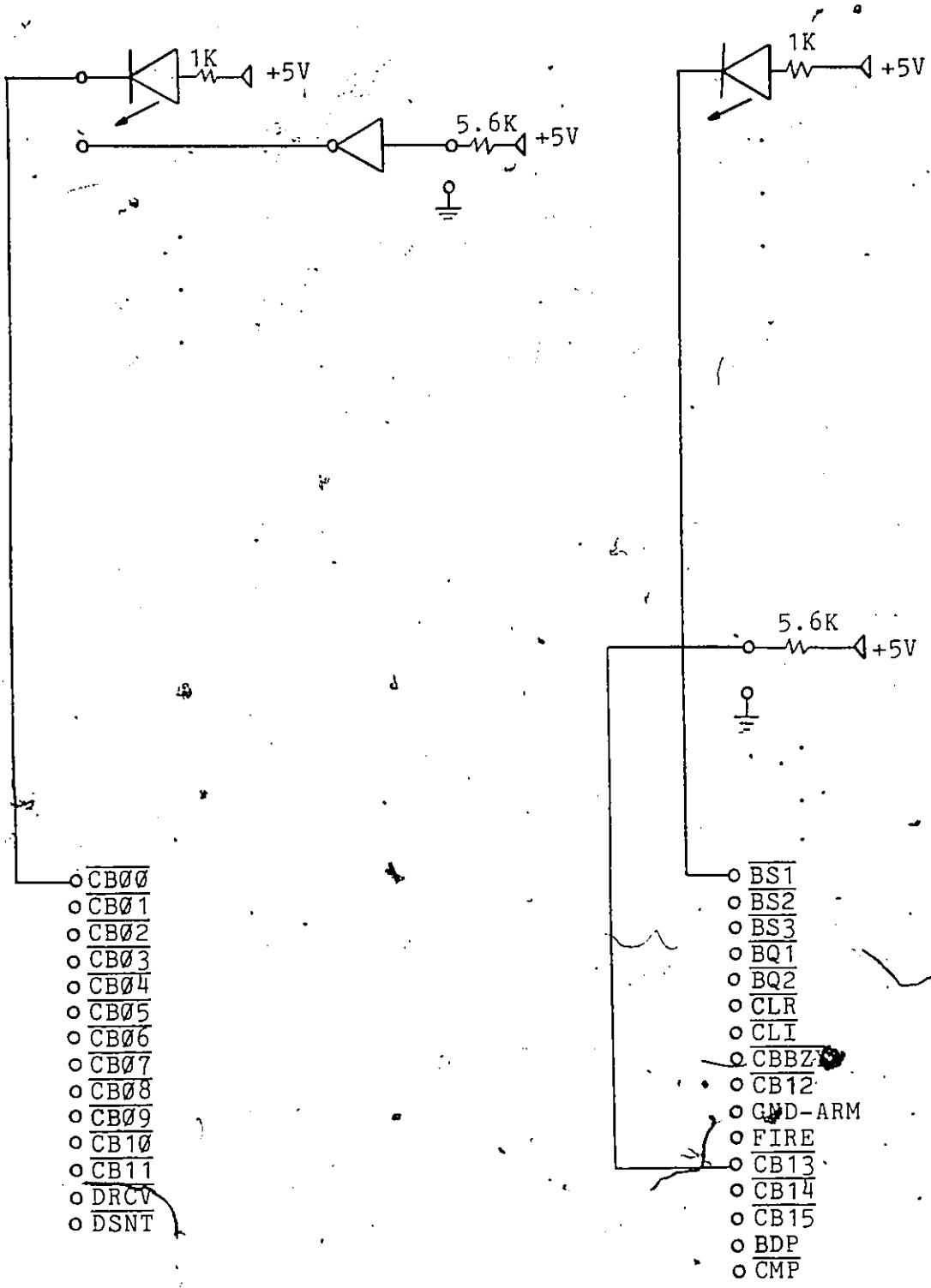


Figure 16. Simulation board

9. TEST RESET
10. SYSTEM RESET
11. PAUSE
12. Display mode
13. Digital mode
14. UNDERLOAD
15. OVERLOAD
16. MALFUNCTION

The results demonstrated in figure 17 show that system performance is satisfactory and all requirements are met. Figure 18 illustrates the testing results of diagnostic software with the following specifications:

INCREMENTAL VOLTAGE D = 10.0 KV

CUMULATIVE DISTRIBUTION FUNCTION P = 0.1

LEVEL OF SIGNIFICANCE, ALPHA = 0.05

TOLERANCE = 5.0 KV

ESTIMATE OF STANDARD DEVIATION = 10.0 KV

NEW INCREMENT D(NEW) = 15.0 KV

```
.123 456 000 0 0
.123 000 456 0 0
.000 123 456 0 0
.123 456 000 1 1
.123 456 000 1 0
.100 052 010 01

0 000 100 001
0 000 200 002
0 000 300 003
0 000 400 004
0 000 500 005
X 000 600 001

X 001 550 001
X 002 498 002
X 003 446 003
0 004 394 001
0 005 446 002
0 006 498 003
X 007 550 004
0 008 498 004
X 009 550 005
X 010 498 006
&

.548 111 020 0 0
C.ee0Y
.548 111 020 0 0

X 000 548 001
X 000 448 002
0 000 348 001

0 001 398 001
X 002 509 001
X 003 398 002
X 004 287 003
X 005 176 004
X 006 065 005
UNDERLOAD
&

.421 098 016 0 0

0 000 421 001
0 000 521 002
X 000 621 001

X 001 571 001
0 002 473 001
0 003 571 002
0 004 669 003
0 005 767 004
0 006 865 005
0 007 963 006
OVERLOAD
&

.638 194 010 0 0

0 000 638 001
X 000 738 001

X 001 688 001
0 002 494 001
.237 096 020 0 0

X 000 237 001
X 000 137 002
X 000 037 003

X 001 050 001
UNDERLOAD
&

.592 020 010 0 0

0 000 592 001
0 000 692 002
0 000 792 003
0 000 892 004
0 000 992 005

X 001 992 001
X 002 972 002
X 003 952 003
X 004 932 004
0 005 912 001
0 006 932 002
X 007 952 005
X 008 932 006
0 009 912 003
0 010 932 004
&

.496 073 010 1 0

0 000 496 001
0 000 596 002
X 000 696 001

X 001 646 001
X 002 573 002
X 003 500 003
X 004 427 004
X 005 354 005
0 006 281 001MALFUNCTION
```

Figure 17. Sample testing results

```
O 000 050 001
X 000 150 001

O 001 100 001
O 002 200 002
X 003 300 001
X 004 200 002
O 005 100 003
X 006 200 003
O 007 100 004
O 008 200 005
O 009 300 006
O 010 400 007
X 011 500 004
X 012 400 005
X 013 300 006
O 014 200 008
O 015 300 009
X 016 400 007
X 017 300 008
X 018 200 009
O 019 100 010
O 020 200 011
X 021 300 010
X 022 200 011
O 023 100 012
O 024 200 013
X 025 300 012
&
```

CHARGING (KV)	I	N(I)	I*N(I)	I*I*N(I)
20.0	0	4	0	0
30.0	1	5	5	5
40.0	2	2	4	8
50.0	3	1	3	9
		N	A	B
		12	12.	22.

		MEAN	STANDARD DEVIATION	100P% POINT
ESTIMATE OF	*	25.000	13.970	7.0907
ESTIMATE OF STANDARD DEVIATION OF	*	3.8690	6.1261	8.7550
95.00% CONFIDENCE LIMITS OF	*	8.5157	13.484	19.270
NEW SAMPLE SIZE BASED ON	*	44	65	152

Figure 18. Sample results of diagnostic software

CHAPTER SIX

CONCLUSIONS AND SUGGESTIONS FOR FUTURE WORK

A low hardware investment design for a microprocessor-based controller for an impulse generator has been presented in this thesis. The unit constructed is very versatile. Basically the hardware is used for I/O expansions and all of the control and data handling features are implemented by means of firmware. The resulting system can be easily adapted for other applications simply by modifying the firmware. In the case of impulse testing, additional PROM and RAM boards enable expansions to include features, such as, on-site data analysis, polarity selection, testing with varying increments, adjustable sphere gap control, minimum 50% flashover voltage, peak voltage, flashover time and time to crest.

Even though the operations of the unit has been verified only under simulation conditions, it is expected that performance of the system will not deviate from the specified requirements in an actual operating environment when proper shielding from interference and proper signals from corresponding units are provided.

APPENDIX A

CONTROL FIRMWARE PROGRAM

```
 CR     =    370
TO      =    379
TI      =    408
IRP     =    613
CP0     =    586
HEX     =    618
D3M     =    236
CV      =    288
        =    0
/*****INITIALIZE ALL OUTPUT PORTS & RAM POINTER
        NOP
        NOP
        FIM   10    0       /CLEAR CHARG. VOLT. &
        SRC   10            /R7912 COMMAND LINES
        LDM   8
        WRR
        LDM   11            /ENABLE CHARG. VOLT REGS
        WRR                 /& R7912 COMMAND LINES
        XCH   10            /SET CLR TO INITIALIZE R7912
        SRC   10            /& ITS INTERFACE
        LDM   6             /DISABLE CLEAR INTERRUPT
        WMP
        FIM   10    32
        SRC   10            /CLEAR ALL FLIP-FLOPS
        LDM   0             /AND READY-OUT
        WRR
        LDM   10            /ENABLE FLIP-FLOPS
        WRR
        INC   10            /SET PAUSE-OUT & TV-OUT
        SRC   10            /SYSTEM RESET LIGHT ON
        LDM   13
        WRR
        LDM   14
        XCH   10            /RESET GND ARM, FIRE, CBBZY & CB12
        SRC   10
        LDM   6
        WMP
        LDM   0             /RESET LAMPS
        WRR
        FIM   8     0       /SET RAM LOAD POINTER TO 0
/*****INPUT SPECS FROM TTY & LOAD DATA INTO RAM
        JMS   CR            /BEGIN A NEW LINE
        FIM   2     46      /PRINT '.' INDICATING
        JMS   TO            /READY TO INPUT FROM TTY
GET,    JMS   TI            /GET ONE CHAR FROM TTY
        CLC
        ADD   2             /CHAR='DECIMAL NUMBER'?
        JCN   12    *+19    /NO, PROCEED TO ANOTHER CHECK
        CLC                 /UPPER ORDER BITS CHECKED OUT
        LDM   6             /CHECK LOWER ORDER BITS
        ADD   3
        JCN   2     GET     /NO, GET NEXT CHAR
        CLC
        LDM   5             /YES, FIRST 11 DECIMAL DIGITS
```

```
        ADD   9              /ALREADY OBTAINED?
        JCN   6      GET     /YES, GET NEXT CHAR
        SRC   8              /NO, STORE DATA INTO RAM
        LD    3
        WRM
        JMS   IRP            /INCREMENT RAM POINTER
        JUN   GET            /GET NEXT CHAR
        CLB                  /CHAR='RETURN'?
        ADD   2
        JCN   12     GET     /NO, GET NEXT CHAR
        LDM   3
        ADD   3
        JCN   12     GET     /NO, GET NEXT CHAR
/*****CHECK IF SPECS ARE VALID
        FIM   8      0       /SPECS LOADING COMPLETED
        JMS   CP0            /C=0, OR D=0, OR N=0?
        JCN   10     0       /YES, RESTART
        JMS   IRP
        ISZ   5      *-2
        ISZ   3      *-8
/*****ADJUST D FOR PROPER INCREMENT
        FIM   8      3       /NO, CONVERT D TO HEX
        JMS   HEX
        FIM   10     5       /SET D=-D
        SRC   10
        LD    15             /GET TWO'S COMPLEMENT
        CMA                  /OF LSD
        IAC
        WRM                  /STORE IN RAM
        FIM   10     4
        SRC   10
        LD    6              /GET ONE'S COMPLEMENT
        CMA                  /OF MIDDLE DIGIT
        JCN   10     *+3     /IF CARRY FROM LSD,
        IAC                  /INCREMENT BY 1
        WRM                  /STORE IN RAM
        FIM   10     3
        SRC   10
        LD    7              /GET ONE'S COMPLEMENT
        CMA                  /OF MSD
        JCN   10     *+3     /IF CARRY FROM MIDDLE
        IAC                  /DIGIT, INCREMENT BY 1
        WRM                  /STORE IN RAM
/*****CHECK AUTOMATIC & DELAY OPTION
        FIM   8      9
        FIM   10     224     /SET OUTPUT PORT POINTER
        LDM   0              /INITIALIZE LAMP STATE
        XCH   5
        SRC   8
        RDM                  /FULLY AUTOMATIC?
        JCN   4      *+6     /NO, GO TO CHECK DELAY
        SRC   10             /YES, AUTO LIGHT ON
        LDM   2
        WRR
```

```
        XCH   5           /RESTORE STATE
        INC   9           /DELAY WANTED?
        SRC   8
        RDM
        JCN   4     LGA   /NO, GO TO LOWER GND ARM
        SRC   10          /YES, DELAY LIGHT ON
        LD    5
        IAC
        WRR
        JMS   D3M         /3.00 MIN DELAY
        LD    5           /DELAY LIGHT OFF
        WRR
/*****SET UP GROUNDING ARM
LGA,    JMS   CR          /BEGIN A NEW LINE
        SRC   10
        LDM   4           /LOWER GROUNDING ARM
        WMP
        FIM   6     254   /2.83 SEC DELAY
        JMS   D3M+2
        FIM   8     11    /INITIALIZE K=0,
        FIM   12    7     /B=0, NB=0
        JUN   *+6
/*****INITIALIZE COUNTERS - B, NB, J
        FIM   8     14    /INITIALIZE B=0, NB=0
        FIM   12    10    /SET UP COUNTER TO 6
        SRC   8
        CLB
        WRM               /STORE 0 IN EACH DIGIT
        JMS   IRP         /INCREMENT RAM POINTER
        ISZ   13    *-5   /ALL DIGITS LOADED?
        LDM   11          /YES, INITIALIZE J=-5
        XCH   4           /J=(REG 4)
/*****CHECK CPU RESET, PAUSE & READY STATES
TRY,    JCN   9     0     /TEST=1? YES, RESTART
        LDM   3           /NO, GET STATE OF PAUSE
        XCH   10
        SRC   10
        RDR               /PAUSE WANTED?
        WRR               /RESTORE STATE
        RDR
        RAR               /YES, LOOP UNTIL SWITCH
        JCN   10    *-2   /IS PUSHED AGAIN
        FIM   10    9     /NO, FULLY AUTOMATIC?
        SRC   10
        RDM
        JCN   12    EP0   /YES, GO TO INIT. R7912
        LDM   2
        XCH   10
        SRC   10
        LDM   14          /NO, READY LIGHT ON
        WRR
        INC   10
        SRC   10          /GET STATE OF READY
        RDR               /READY TO PROCEED?
```

```
        RAR
        RAR                     /NO, LOOP UNTIL SWITCH
        JCN   2     *-3         /IS PUSHED
        LDM   2                 /YES, READY LIGHT OFF
        XCH   10                /RESET READY LAMP
        SRC   10
        LDM   10
        WRR
        JUN   CV                /GO TO CONVERT C TO HEX
EP0,    JUN   256               /CONTINUE
        NOP
$
D3M     =     236
WRD     =     684
HEX     =     618
DAT     =     568
        =     256
/*****SET UP R7912 FOR AWAITING AN INPUT SIGNAL
        FIM   0     DAT+4 /INITIALIZE R7912 BY
        JMS   WRD         /COMMAND (4000 OCTAL)
        XCH   10
        SRC   10
        RDR               /GET MODE
        RAL               /DISPLAY MODE?
        JCN   2     DIG   /NO, GO TO SET DIGITAL MODE
        FIM   0     DAT+8 /YES, SET TV MODE
        JMS   WRD
        FIM   0     DAT+10/ENABLE DOT GRATICULE
        JMS   WRD
        JUN   ARM         /GO TO ARM SINGLE SWEEP
DIG,    FIM   0     DAT+12/SET DIGITAL MODE
        JMS   WRD
        FIM   0     DAT+14/DISABLE DOT GRATICULE
        JMS   WRD
ARM,    FIM   0     DAT+16/ARM SINGLE SWEEP
        JMS   WRD
/*****OUTPUT CHARGING VOLTAGE & TRIGGER
CV,     FIM   8     0       /CONVERT C TO HEX
        JMS   HEX
        XCH   10            /SET OUTPUT PORT POINTER
        SRC   10
        LD    15            /OUTPUT HEX LSD
        WRR
        INC   10
        SRC   10
        LD    6             /OUTPUT HEX MIDDLE DIGIT
        WRR
        INC   10
        SRC   10
        LD    7             /OUTPUT HEX MSD
        WRR
        LDM   2             /IMPULSE GENERATOR
        XCH   10            /CHARGED UP?
        SRC   10
```

```
        RDR             /NO, LOOP UNTIL
        RAL             /COMPARATOR OUTPUT
        JCN  10   *-2   /DROPS
        FIM  6    251   /YES, 6 SEC DELAY
        FIM  2    195
        JMS  D3M+4
        LDM  2          /RESET BDP FLIP-FLOP
        WRR
        LDM  10         /ENABLE BDP FLIP-FLOP
        WRR
        LDM  0          /CLEAR CHARGING
        XCH  10         /VOLTAGE TO 0
        SRC  10
        LDM  10
        WRR
        LDM  11
        WRR
        LDM  12         /FIRE AT TRIGGERTRON
        XCH  10
        SRC  10
        LDM  0
        WMP
        JUN  512        /CONTINUE
        NOP
        NOP
        NOP
        NOP
        NOP
        NOP
$
BD   =   906
NBD  =   789
     =   512
/*****CHECK BREAKDOWN PULSE
        FIM  2    248   /SET COUNTER TO
        FIM  12   128   /125 MS
        LDM  4          /RESET TRIGGER
        WMP
        LDM  2
        XCH  10
        SRC  10
        RDR             /BREAKDOWN PULSE?
        RAR
        JCN  10   EB3-2 /YES, GO TO B=B+1
        ISZ  13   *-4   /NO, 125 MS OVER?
        ISZ  12   *-6
        ISZ  3    *-8   /NO, LOOP AND CHECK
        ISZ  2    *-10  /BREAKDOWN PULSE
        FIM  10   9     /YES, FULLY AUTOMATIC?
        SRC  10
        RDM
        JCN  4    EB3   /NO, GO TO NO BREAKDOWN
        LDM  8
        XCH  10
```

```
      SRC   10
      RDR                  /YES, INTERRUPT SIGNAL
      RAR                  /FROM R7912?
      JCN   10    *+6      /YES, GO TO NB=NB+1
      JUN   768            /CONTINUE
      JUN   BD             /GO TO B=B+1
EB3,  JUN   NBD            /GO TO NB=NB+1
      NOP
$
MES   =     473
ID1   =     205
TOM   =     341
CR    =     370
TO    =     379
P3D   =     352
CP0   =     586
TRY   =     166
DD1   =     220
GM3   =     599
      =     768
/*****GENERATOR MALFUNCTION
      ISZ   4     EP3    /NO, J=J+1. J=0? NO, TRY AGAIN
      FIM   0     MES    /YES, SET MESSAGE POINTER
      FIM   6     245    /CHAR COUNTER=11
      JMS   TOM          /PRINT 'MALFUNCTION'
      XCH   10           /MAL LIGHT ON
      SRC   10
      LDM   6
      WRR
      JMS   CR           /NEXT LINE
      LDM   3            /SYSTEM RESET LIGHT ON
      XCH   10
      SRC   10
      LDM   13
      WRR
      JUN   *
/*****NO BREAKDOWN:
NBD,  FIM   10    19     /NB=NB+1
      JMS   ID1
/*****PRINT RESULTS
      JMS   CR           /NEXT LINE
      FIM   2     79     /PRINT '0' INDICATING
      JMS   TO           /NO BREAKDOWN
      FIM   8     11     /PRINT K
      JMS   P3D
      FIM   8     0      /PRINT CHARGING VOLTAGE C
      JMS   P3D
      FIM   8     17     /PRINT TOTAL NUMBER
      JMS   P3D          /OF NON-BREAKDOWN NB
/*****SEARCH FOR ESTIMATE OF STARTING POINT
      FIM   8     11     /K=0?
      JMS   CP0
      JCN   2     NXT+25/NO, GO TO N=N-1
      FIM   8     14     /YES, B=0?
```

```
        JMS   CP0
        JCN   2     NXT+2 /NO, GO TO B>0
        FIM   10    0     /YES, C<90KV?
        SRC   10
        LDM   7
        ADM
        JCN   6     NXT+12/NO, GO TO SET K=1
        RDM               /YES, C=C+10KV
        IAC
        WRM
NXT,    JUN   TRY-2       /DO NEXT TRIAL
        FIM   14    206   /B>0,
        FIM   10    2     /SET C=C+5KV
        JMS   ID1
        ISZ   15    *-4
        ISZ   14    *-6
/*****INITIALIZE TESTING
        FIM   10    13    /SET K=1
        SRC   10
        LDM   1
        WRM
        FIM   10    8     /N=N-1
        JMS   DD1
        JMS   CR          /NEXT LINE
        JUN   TRY-13      /DO NEXT TRIAL
/*****INCREMENT CHARGING VOLTAGE BY D
        FIM   10    8     /K>0,
        JMS   DD1         /N=N-1
        JCN   10    BD-14 /N<0? YES, GO TO STOP
        FIM   10    13    /NO, K=K+1
        JMS   ID1
        JMS   GM3         /SET C=C+D
        FIM   10    2     /C=C+.1KV
        JMS   ID1         /C>99.9KV?
        JCN   2     *+10  /YES, CONTINUE
        ISZ   15    *-6   /NO, COUNTER EXHAUSTED?
        ISZ   14    *-8   /NO, INCREMENT AGAIN
        ISZ   12    *-10
        JUN   TRY-2       /YES, DO NEXT TRIAL
/*****OVERLOAD CHARGING
        JMS   CR          /NEXT LINE
        FIM   0     MES+11
        FIM   6     248   /SET CHAR POINTER
        JMS   TOM         /PRINT 'OVERLOAD'
/*****TESTING COMPLETED AND STOP
        JMS   CR          /NEXT LINE
        FIM   2     38    /PRINT '&' INDICATING
        JMS   TO          /TESTING COMPLETED
        FIM   2     7     /RING BELL
        JMS   TO
        JMS   CR          /NEXT LINE
        JUN   0           /RESTART
/*****BREAKDOWN:
BD,     FIM   10    16    /B=B+1
        JMS   ID1
```

```
/*****PRINT RESULT
      JMS  CR          /NEXT LINE
      FIM  2    88     /PRINT 'X' INDICATING
      JMS  TO          /BREAKDOWN
      FIM  8    11     /PRINT K
      JMS  P3D
      FIM  8    0      /PRINT CHARGING VOLTAGE C
      JMS  P3D
      FIM  8    14     /PRINT TOTAL NUMBER
      JMS  P3D         /OF BREAKDOWN B
/*****SEARCH FOR ESTIMATE OF STARTING POINT
      FIM  8    11     /K=0?
      JMS  CP0
      JCN  2    EP3-34/NO, GO TO K>0
      FIM  8    17     /YES, NB=0?
      JMS  CP0
      JCN  2    *+21   /NO, GO TO NB>0
      FIM  10   0      /YES, C<10KV?
      SRC  10
      RDM
      JCN  4    *+5    /YES, GO TO C<10KV
      DAC              /NO, C=C-10KV
      JUN  NXT-1       /DO NEXT TRIAL
      INC  11          /C<10KV,
      SRC  10
      LDM  5           /SET C=5KV
      WRM
      INC  11
      SRC  10
      CLB
      WRM
      JUN  NXT+12      /GO TO SET K=1
      FIM  14   206    /NB>0,
      FIM  10   2      /SET C=C-5KV
      JMS  DD1
      ISZ  15   *-4
      ISZ  14   *-6
      JUN  NXT+12      /GO TO SET K=1
/*****DECREMENT CHARGING VOLTAGE BY D
      FIM  10   8      /K>0,
      JMS  DD1         /N=N-1
      JCN  10   BD-14  /N<0? YES, GO TO STOP
      FIM  10   13     /NO, K=K+1
      JMS  ID1
      JMS  GM3         /SET C=C-D
      FIM  10   2      /C=C-.1KV
      JMS  DD1         /C<0?
      JCN  10   *+10   /YES, CONTINUE
      ISZ  15   *-6    /NO, COUNTER EXHAUSTED?
      ISZ  14   *-8    /NO, DECREMENT AGAIN
      ISZ  12   *-10
      JUN  TRY-2       /YES, DO NEXT TRIAL
/*****UNDERLOAD CHARGING
      JMS  CR          /NEXT LINE
```

```
        FIM  0    MES+19/SET CHAR POINTER
        FIM  6    247   /PRINT 'UNDERLOAD'
        JUN  BD-16
EP3,    JUN  TRY
        NOP
        NOP
        NOP
        NOP
        NOP
        NOP
        NOP
        NOP
        NOP
        NOP
        NOP
        NOP
        NOP
        NOP
        NOP
        NOP
$
DRP     =    501
        =    205
/
/*****ID1: INCREMENT 3-DIG DECI NUMBER BY 1
ID1,    LDM  13           /SET COUNTER TO 3
        XCH  5
        SRC  10
        RDM               /GET ONE DIGIT
        IAC               /INCREMENT BY 1
        DAA               /DECIMAL ADJUSTMENT
        WRM               /RESTORE DIGIT
        JCN  10  *+7      /OVERFLOW? NO, RETURN
        JMS  DRP          /YES, DECREMENT RAM POINTER
        ISZ  5   ID1+2    /GET NEXT DIGIT
        STC               /SET FLAG
        BBL  2
/
/*****DD1: DECREMENT A 3-DIG DECI NUMBER BY 1
DD1,    LDM  13           /SET COUNTER TO 3
        XCH  5
        SRC  10
        RDM               /GET ONE DIGIT
        DAC               /DECREMENT BY 1
        WRM               /RESTORE DIGIT
        JCN  2    *+9     /NEED BORROW? NO, RETURN
        TCS               /YES, SET DIGIT=9
        WRM               /RESTORE DIGIT
        JMS  DRP          /DECREMENT RAM POINTER
        ISZ  5    DD1+2   /GET NEXT DIGIT
        CLC
        BBL  0
/
```

```
/*****D3M: 3.00 MIN DELAY
D3M,   FIM   6     129
       FIM   2     0
       FIM   12    0
       ISZ   13    *
       ISZ   12    *-2
       ISZ   3     *-4
       ISZ   2     *-6
       ISZ   7     *-8
       ISZ   6     *-10
       BBL   0
       NOP
$
IRP    =     613
       =     341
/
/*****TOM: PRINT A MESSAGE
TOM,   FIN   2             /GET ONE CHAR
       JMS   TO            /OUTPUT ONE CHAR
       ISZ   1     *+3     /INCREMENT CHAR
       INC   0             /POINTER
       ISZ   7     *-6     /WHOLE MESSAGE PRINTED?
       ISZ   6     *-8     /NO, OUTPUT NEXT CHAR
       BBL   14            /YES, RETURN
/
/*****P3D: PRINT A 3-DIGIT DECI NUMBER
P3D,   LDM   13            /SET COUNTER TO 3
       XCH   5
       FIM   2     32      /BLANK
       JMS   TO
       LDM   3             /SET DECIMAL
       XCH   2             /HIGHER ORDER BITS
       SRC   0
       RDM                 /GET DECIMAL
       XCH   3             /LOWER ORDER BITS
       JMS   TO            /PRINT NUMBER
       JMS   IRP           /INCREMENT RAM POINTER
       ISZ   5     P3D+6   /GET NEXT DIGIT
       BBL   0             /NUMBER PRINTED, RETURN
/
/*****CR: BEGIN A NEW LINE
CR,    FIM   2     13      /'CARRIAGE RETURN'
       JMS   TO
       FIM   2     10      /'LINE FEED'
       JMS   TO
       BBL   0
/
/*****TO: OUTPUT ONE CHAR TO TTY, CHAR=(REG 2, 3)
TO,    FIM   12    0       /SET UP PORT 0
       SRC   12
       CLB
       WMP                 /WRITE START BIT
       LDM   8             /SET BIT COUNTER TO 8
       XCH   4             /REG 4 = BIT COUNTER
```

```
TO1,  JMS  MS9        /9.09 MS DELAY
      CLC
      XCH  2          /SHIFT 8 BITS RIGHT
      RAR
      XCH  2
      XCH  3
      RAR
      XCH  3
      TCC             /CARRY TO ACC
      WMP             /OUTPUT BIT TO TTY
      ISZ  4   TO1    /CONTINUE LOOPING
      JMS  MS9        /9.09 MS DELAY
      LDM  1          /WRITE STOP BIT 1
      WMP
      JMS MS9         /9.09 MS DELAY
      JMS MS9         /AND ANOTHER
      BBL  0
/
/*****TI: INPUT ONE CHAR. FROM TTY, CHAR=(REG 2, 3)
TI,   FIM  6    64    /SET UP RAM PORT 1
      SRC  6
      LDM  0          /WRITE 0 AT RAM PORT 1 BIT 0
      WMP             /TO ENABLE TAPE READER
      FIM  2    0     /INITIALIZE WORKING REGISTERS
      LDM  8          /SET COUNTER TO 8
      XCH  4          /REG 4 =BIT COUNTER
      FIM  12   0     /SET UP PORT 0
      SRC  12
      RDR             /READ FROM KEYBOARD
      RAR             /SHIFT TO CARRY
      JCN  10   *-2   /LOOP WAITING FOR START BIT
      JMS  MS4        /4.55 MS DELAY
      SRC  6
      LDM  1          /WRITE 1 AT RAM PORT 1 BIT 0
      WMP             /TO TURN READER OFF
      SRC  12
      CLB             /WRITE 0 INTO RAM PORT 0
      WMP             /TO ECHO START BIT
TI1,  JMS  MS9        /9.09 MS DELAY
      RDR             /INPUT DATA
      CMA             /COMPLEMENT ACC
      WMP             /ECHO DATA BIT
      RAR             /BIT TO LINK
      LD   2          /GET UPPER NIBBLE
      RAR             /SHIFT IN CARRY
      XCH  2          /SAVE UPPER NIBBLE
      LD   3          /GET LOWER NIBBLE
      RAR             /SHIFT IN CARRY
      XCH  3          /SAVE LOWER NIBBLE
      ISZ  4    TI1   /GET ALL 8 BITS
      JMS  MS9        /YES, WAIT FOR STOP BIT 1
      LDM  1
      WMP             /ECHO STOP BIT 1
      JMS  MS9        /9.09  MS DELAY
```

```
        JMS   MS4          /4.55 MS DELAY
        XCH   2            /ELIMINATE PARITY BIT
        RAL
        CLC                /CLEAR MOST SIGNIFICANT BIT
        RAR
        XCH   2            /INPUT ONE CHAR FROM TTY COMPLETED
        BBL   13           /RETURN
/
/*****MS9: 9.09 MS DELAY
/*****MS4: 4.55 MS DELAY
MS9,    FIM   14    60     /9.09 MS DELAY
        ISZ   15    *
        ISZ   14    *-2
MS4,    FIM   14    60     /4.55 MS DELAY
        ISZ   15    *
        ISZ   14    *-2
        BBL   0
/
/*****MESSAGES
MES,    77                 / 'M'
        65                 / 'A'
        76                 / 'L'
        70                 / 'F'
        85                 / 'U'
        78                 / 'N'
        67                 / 'C'
        84                 / 'T'
        73                 / 'I'
        79                 / 'O'
        78                 / 'N'
        79                 / 'O'
        86                 / 'V'
        69                 / 'E'
        82                 / 'R'
        76                 / 'L'
        79                 / 'O'
        65                 / 'A'
        68                 / 'D'
        85                 / 'U'
        78                 / 'N'
        68                 / 'D'
        69                 / 'E'
        82                 / 'R'
        76                 / 'L'
        79                 / 'O'
        65                 / 'A'
        68                 / 'D'
/
/*****DRP: DECREMENT RAM POINTER
DRP,    LD    11           /DECREMENT LOWER ORDER
        DAC                /POINTER BY 1;
        XCH   11           /IF NO BORROW,
        JCN   2     *+5    /PROCEED TO EXIT
        LD    10           /IF BORROW REQUIRED
```

```
        DAC             /DECREMENT HIGHER ORDER
        XCH  10         /POINTER BY 1
        SRC  10
        BBL  0
        NOP
$
D3M     =    236
        =    568
/
/*****FACTORS & COMMAND
DAT,    154             /C/IC=00, FACTOR=9A
        160             /C/IC=01, FACTOR=A0
        250             /C/IC=10, FACTOR=FA
        0               /C/IC=11, FACTOR=00
        7               /COMMAND=4000
        255             /INITIALIZE R7912
             @D3M    =    236
        =    568
/
/*****FACTORS & COMMAND
DAT,    154             /C/IC=00, FACTOR=9A
        160             /C/IC=01, FACTOR=A0
        250             /C/IC=10, FACTOR=FA
        0               /C/IC=11, FACTOR=00
        7               /COMMAND=4000
        255             /INITIALIZE R7912
        11              /COMMAND=2020
        239             /READ STATUS WORD
        11              /COMMAND=2005
        250             /SET R7912 TO TV MODE
        11              /COMMAND=2014
        243             /ENABLE DOT GRATICULE
        11              /COMMAND=2015
        242             /SET R7912 TO DIGITAL MODE
        11              /COMMAND=2004
        251             /DISABLE DOT GRATICULE
        11              /COMMAND=2040
        223             /ARM SINGLE SWEEP
/
/*****CP0: COMPARE A 3-DIGIT NUMBER WITH 0
CP0,    STC             /SET FLAG
        LDM  13         /SET COUNTER=3
        XCH  5
        SRC  8
        RDM             /GET ONE DIGIT
        JCN  12   *+7   /DIGIT=0?NO, RETURN
        JMS  IRP        /YES, INCREMENT RAM POINTER
        ISZ  5    *-6   /GET NEXT DIGIT
        CLC             /CLEAR FLAG
        BBL  0
/
/*****GM3: GET 3 DIGITS FROM RAM
GM3,    FIM  8    3
        SRC  8
```

```
        RDM             /GET D AS COUNTER
        XCH  12         /GET MSD
        JMS  IRP        /INCREMENT POINTER
        RDM             /GET MIDDLE DIGIT
        XCH  14
        JMS  IRP        /INCREMENT POINTER
        RDM             /GET LSD
        XCH  15
        BBL  0
/
/*****IRP: INCREMENT DATA RAM POINTER
IRP,    ISZ  9    *+3
        INC  8
        SRC  8
        BBL  0
/
/*****HEX: CONVERT FROM DECI TO HEX, HEX=(REG 7,6,5)
HEX,    FIM  6    0     /INITIALIZE HEX MS 2 DIGITS=00
        SRC  8
        RDM             /GET DECI MSD
        XCH  12
        JMS  IRP        /INCREMENT RAM POINTER
        RDM             /MSD OF AUGEND =
        XCH  14         /DECI MIDDLE DIGIT
        JMS  IRP        /INCREMENT RAM POINTER
        RDM             /LSD OF AUGEND =
        XCH  15         /DECI LSD
        FIM  2    234   /ADDEND = -16
        FIM  0    DAT   /SET STATUS FACTOR POINTER
        JMS  AD         /GET SUM OF THE TWO NUMBERS
        JCN  2    *+7   /ANY BORROW? IF NOT, PROCEED
        LD   12         /YES, BORROW 1 FROM DECI MSD
        DAC
        JCN  10   *+11  /IS DECI MSD NEGATIVE?
        XCH  12         /NO, STORE DECI MSD
        FIN  2          /ADDEND=STATUS FACTOR
        JMS  AD         /DECIMAL ADJUSTMENT OF SUM
        ISZ  6    *+3   /INCREMENT HEX MIDDLE DIGIT
        INC  7          /IF >F, INCREMENT HEX MSD
        JUN  *-19       /PERFORM SUBTRACTION AGAIN
        FIM  2    6     /DECI NUMBER < 16,
        JMS  AD         /RESTORE HEX LSD
        JCN  10   *+6   /DECI NUMBER > 9?
        FIM  2    10    /YES, ADJUST HEX LSD
        JMS  AD         /BY ADDING 10
        BBL  11         /NO, RETURN
/
/*****AD: ADD 2 NOS. OF 8 BITS, SUM=(REG 4, 5)
AD,     CLC
        LD   15         /GET LSD OF AUGEND
        ADD  3          /ADD LSD OF ADDEND
        XCH  15         /STORE PARTIAL SUM
        JCN  10   *+5   /INTERMEDIATE CARRY = 0?
        ISZ  1    *+3   /NO, INCREMENT STATUS
```

```
        INC   0
        LD    14          /YES, GET MSD OF AUGEND
        ADD   2           /ADD MSD OF ADDEND
        XCH   14          /STORE PARTIAL SUM
        JCN   10    *+6   /CARRY=0?
        ISZ   1     *+3   /NO, INCREMENT STATUS TWICE
        INC   0
        ISZ   1     *+3
        INC   0
        BBL   0           /YES, RETURN
/
/*****WRD: WRITE A COMMAND TO R7912
WRD,    JMS   BUS         /SET CBBZY
        XCH   10          /SET BQ1 INDICATING
        SRC   10          /R7912 WILL RECEIVE
        LDM   13          /DATA FROM CPU
        WMP
        LDM   1
        WMP
        FIN   12          /GET CB08-CB11
        ISZ   1     *+3   /INCREMENT WORD POINTER
        INC   0
        FIN   14          /GET CB00-CB07
        LD    15          /WRITE CB00-CB03
        WRR
        INC   10
        SRC   10
        LD    14          /WRITE CB04-CB07
        WRR
        INC   10
        SRC   10
        LD    13          /WRITE CB08-CB11
        WRR
        LDM   0           /ENABLE COMMAND
        XCH   10          /LINES DRIVERS
        SRC   10
        LDM   7
        WRR
        JMS   HSK         /DSNT-DRCV HANDSHAKE
        JMS   RHS         /RESET DSNT
        XCH   10          /DISABLE COMMAND LINES
        SRC   10          /DRIVERS
        LDM   11
        WRR
        JMS   RCT         /RESET BQ1
        JMS   RBB         /RELEASE CBBZY
        BBL   3
/
/*****BUS: SET BUS BUSY SIGNAL
BUS,    LDM   11          /CB13 SET?
        XCH   10
        SRC   10
        RDR
        RAR               /YES, WAIT UNTIL
```

```
        JCN  10   *-2    /R7912 IS NOT BUSY
        INC  10          /NO, SET CBBZY INDICATING
        SRC  10          /BUS IS BUSY
        LDM  5
        WMP
        BBL  8
/
/*****RBB: RELEASE BUS BUSY SIGNAL
RBB,    LDM  12          /RELEASE CBBZY
        XCH  10          /INDICATING BUS
        SRC  10          /IS IDLE
        LDM  4
        WMP
        BBL  0
/
/*****RHS: RESET DSNT & DRCV
RHS,    LDM  1           /RESET DSNT & DRCV
        XCH  10
        SRC  10
        LDM  3
        WRR
        BBL  0
/
/*****HSK: 4004-R7912 HANDSHAKE ROUTINE
HSK,    LDM  1           /SET DATA SENT (DSNT)
        XCH  10
        SRC  10
        LDM  1
        WRR
        RDR
        RAR              /WAIT FOR DATA RECEIVED
        JCN  2    *-2    /(DRCV) FROM R7912
        BBL  0
/
/*****RCT: RESET CONTROL LINES
RCT,    LDM  8           /RESET BQ1, BQ2
        XCH  10
        SRC  10
        LDM  0
        WMP
        BBL  0
        NOP
        NOP
        NOP
$
```

```
:100000000000002A002BD8E2DBE2BA2BD6E12A202B13
:10001000D0E2DAE26A2BDDE2DEBA2BD6E1D0E228CA
:10002000005172222E517B5198F1821C3EF1D683F1
:10003000 1227F1D589162729A3E052654027F082BF
:10004000 1C27D3831C272800524A1A005265754C7E
:10005000 7348280 3526A2A052BAFF4F2E02A042BD6
:10006000A6F41A65F2E02A032BA7F41A6EF2E02830
:10007000092AE0D0B529E9147D2BD2E2B56929E936
:10008000148A2BA5F2E250ECA5E251722BD4E126A2
:10009000FE50EE280B2C07409D280E2C0A29F0E07C
:1000A000 52657D9DDBB41900D3BA2BEAE2EAF61A59
:1000B000AD2A092BE91CCAD2BA2BDEE26A2BEAF67A
:1000C000F612BED2BA2BDAE241204100000DDB52B98
:1000D000E9F2FBE01ADB51F575CFFAC2DDB52BE989
:1000E000F8E012EBF9E051F575DE1C0268122004F
:1000F0002C007DF27CF273F272F277F276F2C0009D
:10010000203C52ACBA2BEAF5121420400 52AC20A2EB
:10011000 52AC411C204452AC204652AC204852AC58
:10012000280052 6ABA2BAFE26A2BA6E26A2BA7E23A
:10013000D2BA2BEAF51A3326FB22C350F0D2E2DA05
:10014000E2D0BA2BDAE2DBE2DCBA2BD0E1420000EB
:10015000000000000032517B715B607755765 5CE10
:10016000DDB5222051 7BD3B229E9B3517B526575AD
:10017000 66C0220D517B220A517BC02C002DF0E17C
:10018000D8B451CCF1B2F6B2B3F6B3F7E174825100
:10019000CCD1E151CC51CCC0264027D0E12200D8AF
:1001A000B42C002DEAF61AA451D227D1E12DF0E1AA
:1001B00051CCEAF4E1F6A2F6B2A3F6B374B051CC96
:1001C000D1E151CC51D2B2F5F1F6B2CD2E3C7FCE79
:1001D0007ECE2E3C7FD47ED4C04D414C46554E43FE
:1001E00054494F4E4F5645524C4F414455 4E44454D
:1001F000524C4F4144ABF8BB12FDAAF8BA2BC000D9
:10020000 22F82C80D4E1D2BA2BEAF61A247D097C9C
:10021000097309720 92A092BE91426D8BA2BEAF6C0
:10022000 1A264300438A43150000000000000000026
:1002300000000000000000009AA0FA0007FF0BEF8A
:10024000 0BFA0BF30BF20BFB0BDFFADDB529E91C04
:10025000 5652657 54DF1C0280329E9BC5265E9BEC7
:10026000 5265E9BFC07968 6829C0260029E9BC52F7
:10027000 65E9BE5265E9BF22EA203852971284AC84
:10028000F81A8CBC32529776 8A674272206529 7C8
:10029000 1A96220A5297CBF1AF83BF1AA071A060C1
:1002A000AE82BE1AAB71A86071AB60C052D5BA2BDA
:1002B000DDE1D1E13C71B8603EAFE26A2BAEE26AAB
:1002C0002BADE2D0BA2BD7E252ED52E7BA2BDBE2EC
:1002D00052F752E1C3DBBA2BEAF61AD86A2BD5E102
:1002E000C8DCBA2BD4E1C0D1BA2BD3E2C0D1BA2B2F
:1002F000D1E2EAF612F2C0D8BA2BD0E1C000000079
:10030000 74ED20D926F55155BA2BD6E25172D3BAE5
:10031000 2BDDE243132A1350CD517222 4F517B281B
:10032000 0B516028005160281151602 80B524A126D
:10033000 5A280E524A12432A002BD7EB164DE9F2E7
:10034000E040A42ECE2A0250CD7F457E452A0D2BBB
```

```
:10035000D1E02A0850DC517240992A0850DC1A7CFE
:100360002A0D50CD52572A0250CD12747F667E66F8
:100370007C6640A4517220E426F85155517222621
:1003800517B220751 7B51724000 2A1050CD51728F
:10039000225851 7B280B516028005160280E516073
:1003A000280B524A12 B2811524A12BF2A002BE9BD
:1003B00014B5F843406B2BD5E06B2BF0E0434D2E8A
:1003C000CE2A0250DC7FC17EC1434D2A0850DC1A80
:1003D0007C2A0D50CD52572A0250DC1AE57FD77E79
:1003E000D77CD740AA517220EC26F7437A40A60070
:1003F000000000000000000000000000000000FD
:00
```

APPENDIX B

ANALYSIS SOFTWARE PROGRAM

```
C*************************************************************
C*                                                           *
C*       STATISTICAL ANALYSIS OF SENSITIVITY TESTING         *
C*                 USING UP-AND-DOWN METHOD                  *
C*                                                           *
C*************************************************************
C
      DIMENSION CB(1000),CNB(1000),YMIX(1000),
     #  F(31,2),TD(35,12)
      INTEGER X,O,CH
      DATA X/1HX/,O/1HO/
C*******GET SPECIFICATIONS
      TYPE 'TURN TAPE READER AND LINE PRINTER ON.'
      ACCEPT 'INCREMENTAL VOLTAGE D (IN KV) = ',D
      ACCEPT 'CUMULATIVE DISTRIBUTION FUNCTION P = ',P
      ACCEPT 'LEVEL OF SIGNIFICANCE ,ALPHA = ',ALPHA
      TYPE 'FOR DETERMINING NEW SAMPLE SIZE :'
      ACCEPT 'TOLERANCE = ',T
      ACCEPT 'ESTIMATE OF STANDARD DEVIATION = ',SIGMA
      ACCEPT 'NEW INCREMENT, D(NEW) (IN KV) = ',DNEW
C*******READ TAPE AND STORE DATA IN FILE
      DELETE 'UDATA'
      OPEN 0, 'STTR1'
      OPEN 1, 'UDATA'
   50 READ(0,END=54) CH
      WRITE(1) CH
      WRITE(12) CH
      GO TO 50
   54 CLOSE 0
      CLOSE 1
C*******REARRANGE DATA ACCORDING TO SYMBOL
      OPEN 1, 'UDATA'
      I=1
      J=1
      CMAX=0.0
      CMIN=99.9
    1 READ(1,100,ERR=10,END=9) CH,K,IC,IB
  100 FORMAT(S1,3I4)
      IF(CH.EQ.X)GO TO 3
      IF(CH.EQ.O)GO TO 6
   10 GO TO 1
C*******BREAKDOWNS
    3 IF(K.EQ.0)GO TO 1
      CB(I)=IC*0.1
      I=I+1
      IF(CB(I).LE.CMAX)GO TO 4
      CMAX=CB(I)
    4 IF(CB(I).GE.CMIN)GO TO 1
      CMIN=CB(I)
      KMIN=1
      GO TO 1
C*******NON-BREAKDOWNS
    6 IF(K.EQ.0)GO TO 1
      CNB(J)=IC*0.1
```

```
            J=J+1
            IF(CNB(J).LE.CMAX)GO TO 8
            CMAX=CNB(J)
        8   IF(CNB(J).GE.CMIN)GO TO 1
            CMIN=CNB(J)
            KMIN=-1
            GO TO 1
C*******SORT OUT SYMBOL WITH LESS OCCURRENCE
        9   CLOSE 1
            DELETE 'UDATA'
            IF(J.LT.I)GO TO 12
            N=I-1
            ISYM=1
            DO 11 I1=1,N
       11   YMIX(I1)=CB(I1)
            GO TO 14
       12   N=J-1
            ISYM=-1
            DO 13 I1=1,N
       13   YMIX(I1)=CNB(I1)
C*******GET FREQUENCY AT EACH LEVEL AND TABULATE
       14   Y0=99.9
            YN=0.0
            DO 15 I1=1,N
            IF(YMIX(I1).LT.Y0)Y0=YMIX(I1)
            IF(YMIX(I1).GT.YN)YN=YMIX(I1)
       15   CONTINUE
            WRITE(12,106)
      106   FORMAT('0','CHARGING (KV)     I    N(I)',
           #  '    I*N(I)   I*I*N(I)')
            A=0.0
            B=0.0
            I=0
       16   NI=0
            DO 17 I1=1,N
            IF(YMIX(I1).EQ.Y0)NI=NI+1
       17   CONTINUE
            IF(I.EQ.0)YO=Y0
            IN=I*NI
            ISQN=I*IN
            A=A+IN
            B=B+ISQN
            WRITE(12,107) Y0,I,NI,IN,ISQN
      107   FORMAT(' ',4X,F5.1,6X,I3,3X,I3,3X,I6,2X,I8)
            IF(Y0.GE.YN)GO TO 19
            Y0=Y0+D
            I=I+1
            GO TO 16
       19   WRITE(12,108) N,A,B
      108   FORMAT('0',23X,'N',8X,'A',9X,'B'/
           #  22X,I3,F10.0,F10.0)
C*******DATA ANALYSIS USING FORMULAS OF UP-AND-DOWN METHOD
            HALPHA=ALPHA/2.0
            RN=N
```

```
      RN1=RN-1.0
      OPEN 0, 'NORMAL'
      READ(0,109) ((F(I,J),J=1,2),I=1,31)
109   FORMAT(2F10.4)
      CLOSE 0
      OPEN 1, 'TDIST'
      READ(1,110) ((TD(I,J),J=1,12),I=1,35)
110   FORMAT(12F10.4)
      CLOSE 1
      DO 21 I=1,31
      IF(P.EQ.F(I,1))GO TO 22
      IF(P.GT.F(I,1).AND.P.LT.F(I+1,1))GO TO 23
 21   CONTINUE
 22   ZP=F(I,2)
      GO TO 24
 23   ZP=(F(I,2)+F(I+1,2))/2.0
 24   DO 25 J=2,12
      IF(HALPHA.GE.TD(1,J))GO TO 26
 25   CONTINUE
 26   DO 27 I=2,35
      IF(RN1.LE.TD(I,1))GO TO 28
 27   CONTINUE
 28   R=1.0
      IF(ISYM.EQ.KMIN)R=1.0
      YBAR=YO+D*(A/RN+R/2.0)
      S=1.62*D*((RN*B-A*A)/(RN*RN)+0.029)
      S100P=YBAR+ZP*S
      SYBAR=(6.0*S+D)/(7.0*RN**0.5)
      SS=(1.1*S+0.3*S*S/D)/RN**0.5
      SS100P=(SYBAR*SYBAR+ZP*ZP*SS*SS)**0.5
      CONFY=TD(I,J)*SYBAR
      CONFS=TD(I,J)*SS
      CONFP=TD(I,J)*SS100P
      RNY=((6.0*SIGMA+DNEW)*TD(I,J)/(7.0*T))**2.0*2.0
      RNS=((1.1*SIGMA+0.3*SIGMA**2.0/DNEW)*TD(I,J)/T)**2.0*2.0
      NY=RNY
      NS=RNS
      NP=RNY+RNS*ZP*ZP
      P1=100.0*(1.0-ALPHA)
      WRITE (12,111)
111   FORMAT('0',44X,'MEAN',9X,'STANDARD DEVIATION',3X,
     #'100P% POINT')
      WRITE(12,112) YBAR,S,S100P
112   FORMAT(' ','ESTIMATE OF',25X,'* ',G16.5,2(2X,G16.5))
      WRITE(12,113) SYBAR,SS,SS100P
113   FORMAT(' ','ESTIMATE OF STANDARD DEVIATION OF   *',
     #G16.5,2(2X,G16.5))
      WRITE(12,114) P1,CONFY,CONFS,CONFP
114   FORMAT(' ',F6.2,'% CONFIDENCE LIMITS OF',8X,'*',
     #G16.5,2(2X,G16.5))
      WRITE(12,115)NY,NS,NP
115   FORMAT(' ','NEW SAMPLE SIZE BASED ON',12X,'* ',
     #I10,2(8X,I10))
      STOP
      END
```

APPENDIX C

OPERATING PROCEDURE

OPERATING PROCEDURE

1. Set up equipments according to system configuration chosen. Refer to R7912 manuals for operation of Transient Digitizer.
2. Power up microprocessor-based control unit, Teletype, impulse generator control unit, Transient Digitizer and associate equipments.
3. Push SYSTEM RESET.
4. Type in initial charging voltage, incremental voltage, sample size, automatic and delay options. Note that only the first eleven decimal digits are loaded.
5. If delay is required, DELAY light will stay on for 3 minutes and testing will start after such time lag.
6. For semi-automatic operation, obtain hard copies if desired and push READY when it is lit to initiate next trial.
7. For fully automatic operation, AUTO light will be on throughout the tests. Transient Digitizer can be operated in display or digital mode through pushing the TV switch. When TV is on, it indicates display mode. Transient Digitizer is operated in digital mode when TV is off. MAL is lit if five sequential trials fail.
8. When breakdown occurs, BREAKDOWN will be lit.
9. PAUSE is lit when pushed, and testing activities of the following trial will cease. They will be resumed when PAUSE is pushed again. At the same time PAUSE light

will be off.

10. TEST RESET is lit when pushed. Upon completion of the present trial it will be off and the system will be reinitialized.
11. SYSTEM RESET switch can be used to reinitialize the system at any time. However at certain stage during the tests it is not desirable to perform system reinitialization. This is indicated by SYSTEM RESET not being lit.

APPENDIX D

TELETYPE INPUT/OUTPUT

TELETYPE INPUT/OUTPUT

INPUT FROM TTY

Any number of characters can be typed but only the first eleven decimal digits before a 'carriage return' are loaded.

$D_0D_1D_2$ - initial charging voltage C (.1 - 99.9 KV)

$D_3D_4D_5$ - incremental voltage D (.1 - 99.9 KV)

$D_6D_7D_8$ - sample size M (1 - 999)

D_9 - automatic option (=Ø - semi-automatic, ≠Ø - fully automatic)

D_{10} - delay option (=Ø - no delay, ≠Ø - 3 minutes delay).

OUTPUT TO TTY

O K C NB

X K C B

where "O" indicates no breakdown

"X" indicates breakdown

K - number of tests done (Ø - 999)

C - charging voltage (.1 - 99.9 KV)

NB - number of non-breakdown (Ø - 999)

B - number of breakdown (Ø - 999)

OVERLOAD - C > 99.9 KV

UNDERLOAD - C ≤ Ø KV

MALFUNCTION - Fails for five sequential trials.

& - Testing completed.

APPENDIX E

DESCRIPTION OF FILES

DESCRIPTION OF FILES

DISK FILES

IMPCON.Ø - IMPCON.6: Source files of firmware in INTEL-4 assembly language.

IMPCON.ØL - IMPCON.6L: Binary files of firmware.

IMPCON.R: Hexadecimal file of firmware.

UPDOWN: Source file of diagnostic software in FORTRAN V language.

UPDOWN.SV: Save file of diagnostic software.

UPDOWN.RB: Relocatable binary file of diagnostic software.

NORMAL: Probabilities of Normal Distribution.

TDIST: Probabilities of T-Distribution.

MEMORY MAP OF FIRMWARE

ØØØ - ØCC	IMPCON.Ø
ØCD - ØFF	IMPCON.4
1ØØ - 154	IMPCON.1
155 - 1FF	IMPCON.5
2ØØ - 228	IMPCON.2
229 - 237	All ØØ's
238 - 2FF	IMPCON.6
3ØØ - 3FF	IMPCON.3

APPENDIX F

PARTS LIST

PARTS LIST

IC's

SN7404 - A22, A23

SN7408 - A21

SN7474 - A9, A10

SN7475 - A6

SN74116 - A3, A4, A5

SN74126 - A11, A12, A13, A14, A15, A16, A17, A18, A19, A20

SN74138 - A1, A2

MC1741C - A8

AD7520LD - A7

TRANSISTORS

2N3904 - Q1, Q2, Q3, Q4, Q5, Q6, Q7, Q8, Q10, Q11

2N3906 - Q9

RESISTORS (in ohms, $\frac{1}{4}$W, $\pm$10%)

220 ($\frac{1}{2}$W) - R34

270 ($\frac{1}{2}$W) - R35, R36

470 - R9, R11, R13, R26, R27, R29, R30, R32, R37, R39, R41, R54

1K - R10, R12, R14, R31, R33, R38, R40, R42, R55

3.3K - R28

4.7K - R5, R6, R7, R8

5.6K - R16, R17, R18, R19, R20, R21, R22, R23, R24, R25, R43, R44, R45, R46, R47, R48, R49, R50,

R51, R52, R53

12K - R1, R2, R3, R4, R15

CAPACITORS (±20%)

20 - .047 uF

4 - 1.0 uF

LAMPS

T-1 3/4, 6V, .04A, .03CP - L1, L2, L3, L4, L5

T 3¼, 5V, .09A, .25CP - L6, L7, L8, L9

POWER SUPPLIES (from Standard Power Supplies)

SPS40D12/15 - Dual O/P, 12/15 VDC, 1.2A

SPS90D5/12 - Dual O/P, 5VDC, 6A, 10/12 VDC, 2.5/3.0A

OVERVOLTAGE PROTECTION

OVP-1 - 5.35-32 VDC, $8A_{max}$ continuous shunt current, $80A_{max}$ instantaneous current

OVP-11 - 5-8 VDC, $8A_{max}$ continuous shunt current, $80A_{max}$ instantaneous current

APPENDIX G

PINS LIST

PINS LIST

P1 - 100-pin wire-wrap connector for interface module

P2 - 100-pin wire-wrap connector for processor module

J - 37-pin connector for R7912 Transient Digitizer

T - 8-pin connector for Teletype

B - BNC connector

L - lamp

S - switch

P2	P1	J	T	BLS	Signal name	Signal function
1			4		TTY IN	TTY input
	1			L1	SYS-RST	SYSTEM RESET lamp
2	2				$\overline{\text{TEST}}$	$\overline{\text{TEST}}$ pin
3	3				GND	Ground
4	4				GND	Ground
5					NC	ROM IN 2-1
	5				NC	
6	6			S5	$\overline{\text{READY-IN}}$	ROM IN 3-1
7					NC	ROM IN Ø-1
	7				NC	
8	8				$\overline{\text{DSNT-IN}}$	ROM IN 1-1
9	9				BDP-IN	ROM IN 2-Ø
1Ø	1Ø				$\overline{\text{PAUSE-IN}}$	ROM IN 3-Ø
11					NC	Memory address Ø
12					NC	Memory address 1
13					NC	Memory address 2
14					NC	Memory address 3
15					NC	Memory address 4
16					NC	Memory address 5
17					NC	Memory address 6
18					NC	Memory address 7
	11	1			$\overline{\text{CBØØ}}$	Command/data line
	12	2			$\overline{\text{CBØ1}}$	Command/data line
	13	3			$\overline{\text{CBØ2}}$	Command/data line
	14	4			$\overline{\text{CBØ3}}$	Command/data line
	15	5			$\overline{\text{CBØ4}}$	Command/data line

P2	P1	J	T	BLS	Signal name	Signal function
	16	6			$\overline{CB\emptyset5}$	Command/data line
	17	7			$\overline{CB\emptyset6}$	Command/data line
	18	8			$\overline{CB\emptyset7}$	Command/data line
19	19				C$\emptyset$	CHIP SELECT $\emptyset$
2$\emptyset$	2$\emptyset$				C1	CHIP SELECT 1
21					NC	ROM IN $\emptyset$-3
22					NC	ROM IN 1-3
23					NC	$\overline{\text{MEMORY DATA } \emptyset}$
	21				NC	
	22				NC	
	23	9			$\overline{CB\emptyset8}$	Command/data line
24	24				$\overline{TV\text{-}IN}$	ROM IN 3-3
25					NC	$\overline{\text{MEMORY DATA } 1}$
	25	1$\emptyset$			$\overline{CB\emptyset9}$	Command/data line
26			1		TTY PRINTER	Teletype output
	26			L9	BD	BREAKDOWN lamp
27					NC	$\overline{\text{MEMORY DATA } 3}$
28					NC	ROM IN $\emptyset$-2
29					NC	$\overline{\text{MEMORY DATA } 2}$
3$\emptyset$					NC	ROM IN 1-2
31					NC	$\overline{\text{MEMORY DATA } 5}$
32					NC	ROM IN 2-2
33					NC	$\overline{\text{MEMORY DATA } 4}$
	27	11			$\overline{CB1\emptyset}$	Command/data line
	28				NC	
	29	12			$\overline{CB11}$	Command/data line

P2	P1	J	T	BLS	Signal name	Signal function
	30				NC	
	31			B5	BDP	Breakdown pulse
	32				NC	
	33	14			$\overline{\text{CB13}}$	Status flag
34	34				GND	ROM IN 3-2
35					NC	$\overline{\text{MEMORY DATA 7}}$
	35	15			$\overline{\text{CB14}}$	Data Source flag
36	36				$\overline{\text{DRCV-IN}}$	ROM IN 2-3
37					NC	$\overline{\text{MEMORY DATA 6}}$
	37	16			$\overline{\text{CB15}}$	Data Source flag
38	38				CMP	ROM IN 2-3
39					NC	$\overline{\text{RAM OUT Ø-Ø}}$
40					NC	$\overline{\text{RAM OUT 1-Ø}}$
	39		2		TTY PR	TTY printer
	40		6		TTY RD	TTY reader
41	41				$\overline{\text{OUT}}$	Output control line
42	42				$\overline{\text{EN MON PROM}}$	Monitor PROM enable
43	43				-1ØV	-1ØV supply
44					NC	ROM IN Ø-Ø
	44		3		TTY KB	TTY keyboard
45	45				$\overline{\text{CPU RESET}}$	$\overline{\text{CPU RESET}}$ pin
46	46	27			$\overline{\text{BS3}}$	Unit select line
47					NC	$\overline{\text{CM-RAM 2}}$
48					NC	$\overline{\text{CM-RAM 3}}$
49					NC	$\overline{\text{CM-RAM Ø}}$
50					NC	$\overline{\text{CM-RAM 1}}$

P2	P1	J	T	BLS	Signal name	Signal function
	47			B1	CV	CHARGING VOLTAGE
	48			S1	$\overline{\text{SYSTEM RESET}}$	SYSTEM RESET switch
	49	21			$\overline{\text{DRCV}}$	$\overline{\text{DATA RECEIVED}}$
	50	28			$\overline{\text{DSNT}}$	$\overline{\text{DATA SENT}}$
51	51				I/O 1	I/O bus bit 1
52	52				I/O Ø	I/O bus bit Ø
53	53				I/O 2	I/O bus bit 2
54	54				$\overline{\text{IN}}$	Input control
55					NC	F/$\overline{\text{L}}$
	55			S2	$\overline{\text{TEST RESET}}$	TEST RESET switch
56	56				I/O 3	I/O bus bit 3
57	57	13			$\overline{\text{CB12}}$	$\overline{\text{RAM OUT 3-3}}$
58	58	24			$\overline{\text{CBBZY}}$	$\overline{\text{RAM OUT 3-Ø}}$
59	59			B2	GND ARM	$\overline{\text{RAM OUT 3-1}}$
60	60			B4	FIRE	$\overline{\text{RAM OUT 3-2}}$
61	61				$\overline{\text{DC-CLEAR}}$	ROM OUT Ø-1
62	62				DRO	ROM OUT Ø-2
63	63	19			$\overline{\text{CLR}}$	$\overline{\text{RAM OUT 2-2}}$
64	64				$\overline{\text{CV-CLEAR}}$	ROM OUT Ø-Ø
65	65				DRI	ROM OUT Ø-3
66	66	20			$\overline{\text{CLI}}$	$\overline{\text{RAM OUT 2-3}}$
67	67	22			$\overline{\text{BQ1}}$	$\overline{\text{RAM OUT 2-Ø}}$
68	68	23			$\overline{\text{BQ2}}$	$\overline{\text{RAM OUT 2-1}}$
69	69	26			$\overline{\text{BS2}}$	$\overline{\text{RAM OUT 1-2}}$
70					NC	$\overline{\text{RAM OUT Ø-3}}$
71					NC	ROM OUT 1-2

P2	P1	J	T	BLS	Signal name	Signal function
72					NC	$\overline{\text{DATA 3}}$
	7Ø			S4	TV-IN	TV switch
	71				NC	
	72			S3	PAUSE-IN	PAUSE switch
73	73				$\overline{\text{DRCV-OUT}}$	ROM OUT 1-Ø
74	74				$\overline{\text{DSNT-OUT}}$	ROM OUT 1-1
75					NC	ROM OUT 1-3
76					NC	$\overline{\text{DATA 2}}$
	75				NC	
	76			L2	RESET	TEST RESET lamp
77	77				PAUSE-OUT	ROM OUT 3-Ø
78					NC	ROM OUT 3-1
79					NC	$\overline{\text{SYNC}}$
8Ø					NC	$\overline{\text{DATA 1}}$
	78			L5	READY	READY lamp
	79			L3	TV	TV lamp
	8Ø			L8	MAL	MAL lamp
81	81				$\overline{\text{FF-CL}}$	ROM OUT 2-1
82					NC	ROM OUT 2-Ø
83					NC	$\overline{\text{DATA Ø}}$
	82				NC	
	83			L6	AUTO	AUTO lamp
84	84				READY-OUT	ROM OUT 2-2
85	85				SYS-RST-OUT	ROM OUT 3-2
86	86	25			$\overline{\text{BS1}}$	$\overline{\text{RAM OUT 1-1}}$
87	87				$\overline{\text{BDP-CL}}$	ROM OUT 2-3

P2	P1	J	T	BLS	Signal name	Signal function
88	88				$\overline{4002}$ RESET	RAM reset
89			5		READER CONT	TTY control
	89			L4	PAUSE	PAUSE lamp
90					NC	$\overline{\text{RAM OUT 0-2}}$
91					NC	$\overline{\text{RAM OUT 0-1}}$
	90				-15V	-15V supply
	91				+15V	+15V supply
92	92				TV-OUT	ROM OUT 3-3
93					NC	$\overline{\text{CM-ROM}}$
	93			L7	DELAY	DELAY lamp
94	94				C3	CHIP SELECT 3
95					NC	W
	95			B3	$\overline{\text{CMP}}$	$\overline{\text{CMP}}$ pulse
96	96				C2	CHIP SELECT 2
97					NC	$\overline{02}$ CLOCK
98					NC	$\overline{01}$ CLOCK
	97				NC	
	98				NC	
99	99				+5V	+5V supply
100	100				+5V	+5V supply
		17			GND	Ground
		18			GND	Ground
		29			GND	Ground
		30			GND	Ground
		31			GND	Ground
		32			GND	Ground

P2	P1	J	T	BLS	Signal name	Signal function
		33			GND	Ground
		34			GND	Ground
		35			GND	Ground
		36			GND	Ground
		37			GND	Ground
			7		NC	
			8		NC	

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